



EasyGX



Ver: 1.0

Cytech Technology A Macnica Company www.cytech.com 2013-04-25









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Reversion History

Updated Date	Owner	Reversion	Updated Item
2012-10-29	John Lee	Draft 1.0	English edition
2012-02-14	MS	Draft 1.0	Content revised
2013-04-24	John Lee	Draft 1.0	File format adjustment
2013-04-25	John Lee	V1.0	English version released





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1 Introduction



Thank you for your interest in the EasyGX Cyclone[®] IV GX Development Kit. This kit provides a general hardware platform for developing and prototyping low power, high volume, feature rich designs based on Cyclone[®] IV GX transceiver FPGA.

The EasyGX Cyclone[®] IV GX development kit is especially suitable for develop and test PCI Express and 10/100/1000M Ethernet interface, including NIOS II embedded CPU and USB-Blaster function, which provided rich external memory for rapid prototype environment.





1.1 Kit Contents

The EasyGX Cyclone[®] IV GX Development Kit basic package contains:

- Development main board
- USB Blaster expansion board with cable
- USB cable

Optional accessories (not included in basic package):

- PCI-e to 34mm ExpressCard 2.0 adapter
- Other function daughter boards will be released in the future

The picture below is shown for reference; See exact deliverable as standard.



Main board







1.2 Features

- Cyclone[®] IV GX EP4CGX22F324C8N FPGA in 324-pin FineLine BGA (FBGA) package
 - 21,280 LEs
 - 756kb embedded memory, 84 M9K blocks
 - 40 DSP blocks (18x18 bits)
 - PCI Express hard IP block
 - 1.2-V core voltage power
- MAX[®] V 5M80ZE64C5N CPLD in 64-pin plastic Enhanced quad flat pack (EQFP) package
 - 2.5-V core voltage power
- FPGA configuration circuitry
 - MAX V CPLD 5M80Z system controller
 - Embedded on-board USB-Blaster
 - JTAG-based header
 - Erasable programmable configurable serial (EPCS) device
- Transceiver interface
 - PCI Express v1.0 x1 ExpressCard interface
 - 10/100/1000BASE-T Ethernet PHY with RJ-45 connector
 - Two TX/RX transceiver SERDES loopback
- On-Board memeory
 - Micron DDR2 64Mx16 SDRAM MT47H64M16HR-25E:H
 - Altera 16Mb serial flash EPCS16S18N
- Power supply
 - 5V-dc USB input
 - 3.3V-dc PCIe ExpressCard
- Micro-SD card RW supported
- Altera Nios II embedded processor
- IDE base on Eclipse supported
- Include RTOS-Micrium uC/OS-II

1.3 Design Software

Туре	Software		
Logic Design	QUARTUS'II	ModelSim. Altera's version of ModelSim [®] Software	
Embedded Design	Nios' II		
DSP Design	DSP Builder		

Download linkage: http://www.altera.com/products/software/sfw-index.jsp





2 Getting Started

This chapter describes how to install and configure Altera Quartus II software environment

2.1 Software installation

2.1.1 Software introduction

Quartus II software includes everything you need to design Altera FPGA and CPLD families

2.1.1.1 About Quartus version

Web-edition and Subscription-edition is available for downloading via Altera official website. The following will be demonstrated based on Quartus II v12.0 version.

2.1.2 System requirements

2.1.2.1 Hardware requirements

- Windows PC or Linux work station
- Display resolution no less than 768*1024
- Enough hard disk space

2.1.2.2 Interface

- One UART
- USB Host
- 10/100M Ethernet





2.1.3 Installation

2.1.3.1 Download Quartus II software

You can download it from here. There're two methods:

1) Altera Installer

Using Altera Installer, you can download and install the Altera software for Windows or Linux. And you can choose necessary items

Individual software file
 You can download some individual installation packages on the page. You can choose this method if clearly know about what items is needed

2.1.4 Install Quartus II

Procedure below is based on "Altera Installer".

1) Launch "Altera Installer".







- 2) "Altera Installer" leads you to install...
 - a) Agree and click "next" button.

🔮 Altera Installer (12.0 Build 178)	
End User License Agreement To continue installing the soft	ware, you must agree to the terms of the software license agreement below.
	This document contains three separate licensing agreements, identified as "LICENSE.TXT FILE for Nios II v12.0 EDS," "MegaCore Function License Agreement," and "Quartus II, Version 12.0 Standard License Agreement." Acceptance of the terms and conditions of this document serves as an acceptance of each of the three licensing agreements as if they were individually and separately accepted. The terms and conditions of each of the three separate licensing agreements in this document is deemed to be the terms and conditions of a standalone licensing agreement and governs its respective licensing agreements without modifying the terms and conditions of other licensing agreements in this document.
> Introduction > License	The following provision applies to all three licensing agreements below: Altera may store your data and information on its own servers or on servers hosted by third parties. If Altera is providing any software to you for use via the Internet, such software may also be stored on our servers or servers hosted by third parties. For any information, data or software hosted by a third party, although every reasonable effort will be made to keep data and information secure, Altera is not liable for data or information that is inadvertently disclosed by the third party or for any system downtime related to the third party servers.
> Installer Setup	FOR QUARTUS II, VERSION 12.0, ALL DISTRIBUTIONS (WEB DOWNLOAD, CDS, DVDS)
> Select Destination	
> Select Products	QUARTUS II, VERSION 12.0 STANDARD LICENSE AGREEMENT:
> Summary	ALTERA PROGRAM LICENSE SUBSCRIPTION AGREEMENT
> Installation	PLEASE REVIEW THE FOLLOWING TERMS AND CONDITIONS CONTAINED IN THIS ALTERA PROGRAM LICENSE SUBSCRIPTION AGREEMENT (THIS "AGREEMENT")
	$[\ensuremath{\overline{v}}]$ I agree to the terms of the license agreement.
	< Back Next > Cancel

b) If you have not downloaded the installation package, please select as below.

	 Specify the Installation Files Directory Select this option if you want the Altera Installer to retrieve installation files from your hard disk or local network.
	Installer Source Directory: Browse
	Ownload Installation Files from the Internet
Introduction	Select this option if you want the Altera Installer to retrieve installation files from the Internet.
License	Specify how you are connected to the Internet:
Installer Setup	 No proxy (recommended) Manual proxy configuration
Select Destination	Web Proxy: Port:
Select Products	Username:
	Password:
Summary	





c) Choose the installation direction, and pay attention to the hard disk capacity.

Altera Installer (12.0 Build 178)	al O tares Of O Banks O Bank O OF O Color	
Select Destination Specify the software destina	tion directory.	
	Destination Directory:	
	c:\altera\12.0	Browse
	Available Space:	3.6 G
	Temporary Directory for installation files:	
	C:\Users\MORVEN~1\AppData\Local\Temp	Browse
	Available Space:	3.6 G
	Remove saved installation files after completion.	
> Introduction	Download only and install later.	
> introduction	Program Folder	
> License	Specify the Program Folder:	
> Installor Sotup	Altera 12.0 Build 178 (Copy 2)	
	Existing Folders:	
> Select Destination	7-Zip Accessories	<u>^</u>
> Select Products	Acronis Administrative Tools	E
> Summary	Advanced SystemCare 5	
> Summary	Altera 11.1sp2 Build 259	
> Installation	Altera 12.0 Build 178 Altium Designer Summer 09	
		T
	Back N	ext > Cancel

d) Select the devices and items needed.

Altera Installer (12.0 Build 178)	A D term D P	C Standard I	0 mm () mm ()	Index Via	
Select products Select the software products	you want to install.				
	Products			Install Size	Download Size
	 Quartus II Si Ouartus I 	ubscription Editio II software (64-)	on (includes Nios II EDS) pit)	11 G 810 M	7.2 G 122 M
	Device Failed	amilies		6.3 G	6.0 G
	Quartus II W	eb Edition (Free) (includes Nios II EDS)	4.3 G	1.1 G
	ModelSim-Alt	era Starter Editi	on (Free)	3.4 G	409 M
	ModelSim-Alt	era Edition		3.4 G	409 M
//	DSP Builder			254 M	51 M
> Introduction					
> License					
> Installer Setup					
> Select Destination	Description				
> Select Products					~
	Altera Installer 12.	U			-
> Summary					
> Installation		Install:	Download:	_	
> installation	Space Required:	14 G	7.6 G	Se	elect/Deselect All
	Space Available:	3.6 G	3.6 G		
			< Bac	k Next	Cancel





e) Confirm Installation Summary, click Next.

Altera Installer (12.0 Build 178)	1	• X
Installation Summary Review the installation summa	ry to verify your software installation options, and then click Next to begin the installati	on.
	Cache Location: E:\altera_12.0_178	*
	Altera 12.0 Build 178 (Copy 2)	
	Selected Products: Quartus II Subscription Edition (includes Nios II EDS)	
//	 Quartus II Subscription Edition (includes Nios II EDS) Quartus II software (64-bit) 	
> Introduction	• Arria GX • Arria II GX • Arria II GZ • Arria V	
> License	Cyclone Cyclone II	
> Installer Setup	Cyclone II/ III LS Cyclone IV E Cyclone IV GX	=
> Select Destination	• Cyclone V • Legacy Families • MAX TI	
> Select Products	MAX V Stratix	
> Summary	Stratix II GX Stratix II and HardCopy II	
> Installation	Stratix III/IV and HardCopy III/IV Stratix V	
	ModelSim-Altera Starter Edition (Free)	-
	< Back Next > 0	Cancel

f) Download and install.

Please wait while the Altera sof	tware is installed.	
	📩 Downloading Quartus II Subscription Edition (includes Nios II EDS)	0%
All	Products Downloaded Installed	*
	 Quartus II Subscription Edition (includes Nios II EDS) Quartus II Subscription Edition (includes Nios II EDS) Quartus II software (64-bit) Arria GX Arria II GX Arria II GZ Arria V 	E
> Introduction	Cyclone Cyclone II Cyclone III/III LS	
> License > Installer Setup	Cyclone IV E Cyclone IV GX Cyclone V Legacy Families	
> Select Destination	MAX II MAX V Strativ	~
> Select Products	Start Quartus II 12.0	
> Summary	Create Desktop Shortcuts Image: State of the st	
> Installation	☑ ModelSim-Altera Starter Edition (Free)	
	Rate your installation experience	





2.1.5 Acquire license

If you choose free "Web" version, there's no license needed; If you choose "Subscription" version, you need to acquire a license. About how to acquire and activate the license, please purchase subscription license from Altera or authorized distributor.

2.2 Hardware installation

There's no hardware installation needed.





3 Hardware

3.1 Overview

3.1.1 Main board top view



3.1.2 Main board bottom view







3.2 EasyGX hardware – Main board

3.2.1 Main board system block diagram



3.2.2 USB Blaster expansion board diagram







3.2.3 Power supply chain



3.2.4 Function block introduction

3.2.4.1 Power configuration of FPGA

Cyclone IV	SX power requirement.	
Power pin	Voltage (V)	Comments
VCCINT	1.2	Core voltage、Power source of PCI Express
		(PCIe) hardcore IP module and transceiver
		physical coding sublayer (PCS)
VCCA	2.5	PLL analog power supply
VCCD_PLL	1.2	PLL digital power supply
VCCIO	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O power supply
VCC_CLKIN	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	Power supply for differential clock input pin
VCCH_GXB	2.5	Power supply for Transceiver output (TX) buffer
VCCA_GXB	2.5	Power supply for transceiver physical media
		auxiliary sublayer (PMA) and auxiliary
VCCL_GXB	1.2	Power supply for transceiver PMA and auxiliary

Cyclone [®] IV GX power requirement:

- 1) Even if there's no PLL used, VCCA should be powered still.
- I/O bank 3、8 and 9 include configuration pins. You have to power I/O bank 3 and 9 VCCIO to 1.5 V、1.8 V、2.5 V、3.0 V or 3.3 V. As to FPP configuration mode, you should power I/O bank 8 VCCIO to 1.5 V、1.8 V、2.5 V、3.0 V or 3.3 V.
- 3) EP4CGX15、EP4CGX22 (in all package types) and EP4CGX30 (in package F169 and F324) have VCC_CLKIN I/O special for clock input locates on bank 3A and 8A. EP4CGX30 (in F484 package)、EP4CGX50、EP4CGX75、EP4CGX110 and EP4CGX150 (in all package types) have 4 VCC_CLKIN I/Os special for clock input locate on bank 3A、3B、8A and 8B.
- 4) If CLKIN is used as the refclk of high speed serial interface (HSSI), VCC_CLKIN should be set





2.5V. VCC_CLKIN locates on I/O bank 3B and 8B must use 2.5V to support LVDS function, for they are dedicated pins for HSSI refclk. As to EP4CGX50、EP4CGX75、EP4CGX110 and EP4CGX150, single ended input CLK can be used as dedicated input CLK located on I/O bank 3B and 8B.

Power supply configuration schematic of FPGA as below:







3.2.4.2 Ethernet interface

Ethernet connector is showed in the picture blew:



SCH of Ethernet interface:







3.2.4.3 ExpressCard 34 (PCIe) interface

ExpressCard 34 (PCIe) connector is showed in the picture below:





Schematic of ExpressCard 34 (PCIe) connection:







3.2.4.4 Micro-SD

Micro-SD connector is showed in the picture below:

Schematic of Micro-SD:





3.2.4.5 Embedded USB Blaster Function

Schematic of Embedded USB Blaster:



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Embedded USB Blaster jumper (J2) configuration:

J2	USB Blaster Mode	Comment
Shorted	Only for FPGA on board	
Opened	JTAG for FPGA/CPLD off board	Need to connect expansion board to J3





4 Lab Instructions

4.1 Lab 1

4.1.1 Objective

The following lab exercise is to demonstrate LED flashing after complete setup of EasyGX hardware and Quartus II software.

4.1.2 Step by step

Launch Quartus II.







File -> Open Project.

🖞 Quartus II 32-bit					
File	Edit View Project	Assignments P	rocess		
D	New	Ctrl+N	[
2	Open	Ctrl+O	Ē		
	Close	Ctrl+F4	F		
8	New Project Wizard				
8	Open Project	Ctrl+J			
	Save Project				
	Close Project				
	Save	Ctrl+S			
	Save As				
ø	Save All	Ctrl+Shift+	s		
	File Properties		F		
	a		. F		

Find First_design directory, open .qpf file.

Open Project			×
🔾 🖓 🖉 Work (D:)	► Examples First_design	• 😽 搜索 First_de	esign 👂
组织 ▼ 新建文件夹			iii • 🔟 🔞
☆ 收藏夹	名称	修改日期	类型
💠 Dropbox	퉬 db	2012/9/3 15:23	文件夹
🚺 下载	퉬 greybox_tmp	2012/9/3 14:35	文件夹
三 桌面	퉬 incremental_db	2012/9/3 14:35	文件夹
📃 最近访问的位置	🛐 golden_top.qpf	2012/9/1 10:51	QPF 文件
PDproject			
库			
Subversion			
- 视频			
□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □			
☐ 文档			
	III		• •
文件名(N):	▼ Quartus II Pro	oject File (*.qpf 🔻
		tTH(O)	ED:24
		1))(())	#X/H

Click the "Programmer" icon in the toolbar or select Tools->Programmer.







If occur situation below, click "Hardware Setup" on the left-up corner.

👋 Programmer - D:/	Examples/First_design	/golden_top - golde	en_top - [golden	_to 😐 😐	x
File Edit View Pro	ocessing Tools Windo	w Help 🛡			
Hardware Setup	No Hardware	Mode: JTAG	MAX V devices)	Progree	ess:
▶ [™] Start	File	Device	Checksum	Usercode	Progra Config
Stop	golden_top.sof	EP4CGX22CF19	001736A0	FFFFFFF	V
Auto Detect					
Add File					
Change File	<				۰.
Add Device					* =
1 [™] Up					
Down					Ŧ

(🔖 Programmer - D:,	/Examples/First_design/g	golden_top - golder	n_top - [golden	_to 😐 😐	23
	File Edit View Pr	rocessing Tools Window	Help 🛡			
	Hardware Setup	USB-Blaster [USB-0] P to allow background program	Mode: JTAG	MAX V devices)	▼ Progre	ss:
	Mu Start	File	Device	Checksum	Usercode	Progra Config
	Stop	golden_top.sof	EP4CGX22CF19	001736A0	FFFFFFF	V
	Auto Detect					
	X Delete					
	Add File					
1	Change File	•	1			+
1	Save File					-
1	Add Device		<u></u>			=
			A			
	Down					+
						H.





Select "USB_Blaster[USB-0]" in the drop-down box, then click "Close".

Hardware Settings JTAG Settings Select a programming hardware setup hardware setup applies only to the cu Currently selected hardware: USB- Available hardware items	o to use when prog rrent programmer Blaster [USB-0]	ramming devices window.	s. This programming
Hardware USB-Blaster	Server Local	Port USB-0	Add Hardware

Click "Start" in the left to start programming. You can see below if it is successful.

	Mode:	ЛАG	•	Progress:	100%	6 (Successful)	
e	ISP						
	CLAMP						

Once it is programmed successfully, you can see D6~D9 LED flashing in binary-sequential order.







4.2 Lab 2

4.2.1 Objective

The following lab exercise allows you to use NIOS II simple socket server to toggle LED. It also utilized Gigabit Ethernet port as a server controller.

4.2.2 Step by step

Open Examples from "NIOS_demo" folder with project "NIOS_SOC.qpf" in Quartus II

Open Project			×
😋 🕞 🗢 🚺 « Work (D:)	► Examples ► NIOS_demo ► -	← 搜索 NIOS_d	'emo 👂
组织 ▼ 新建文件夹		E	= - 1 🔞
📄 Subversion 🔺	名称	修改日期	类型
副 视频	🃔 .metadata	2012/9/3 14:35	文件夹
	🌗 .qsys_edit	2012/9/3 14:35	文件夹
■ 文档	🌗 db	2012/9/3 15:13	文件夹
📄 迅雷下载 🛛 🔤	🌗 flash	2012/9/3 14:35	文件夹
🚽 音乐	FULL_SYS	2012/9/3 14:35	文件夹
	퉬 greybox_tmp	2012/9/3 14:35	文件夹
🖳 计算机	퉬 incremental_db	2012/9/3 14:35	文件夹
🚢 OS (C:)	鷆 script	2012/9/3 14:35	文件夹
Work (D:)	鷆 software	2012/9/3 14:53	文件夹
Personal (E:)	NIOS_SOC.qpf	2012/5/7 16:56	QPF 文件
👝 Other (F:)			
🚇 CD 驱动器 (H:) 🔻 🗹			•
文件名(1	N):	✓ Quartus II Pro	ject File (*.qpf 🔻
		打开(O)	取消

Then select programmer. Double click the file in the "File" item, choose the file "NIOS_SOC.sof" for programming.



Select New Programming File	×
Look in: D: Examples WIOS_demo	
File name: Files of type: Programming Files (*.sof *.pof *.jam *.jbc *.ekp *.jic)	Open Cancel

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Then, click "Start" to program. Showed as below when it is completed.

Programmer - D:/Examples/NIOS_demo/NIOS_SOC - NIOS_SOC - [NIOS_SOC.cdf]						
File Edit View Pro	ocessing Tools Window	Help 🛡				
Hardware Setup	USB-Blaster [USB-0]	Mode: JTAG		▼ Progre	ss: 00% (Succ	:essful
Enable real-time ISP	to allow background program	ming (for MAX II and N	1AX V devices)			
Start	File	Device	Checksum	Usercode	Program/ Configure	Verify
Stop	NIOS_SOC.sof	EP4CGX22CF19	00D13E9F	FFFFFFF		
Auto Detect						
Delete						
Add File						
	•					•
Save File						<u>^</u>
Add Device						=
The Up						
Down						-

Launch Nios II in the program list, suggest to run it under PC-administrator privilege.





€ N	ios II - ex11/simple_socket_server.h	- Eclipse	
File	Edit Source Refactor Navigat	e Search Run Proj	ect Nios II Window Help
	New	Alt+Shift+N ►	0 - 9 - 10 - 10 - 10
	Open File		simple socket server.h 🛛
	Close	Ctrl+W	
	Close All	Ctrl+Shift+W	Could not open the editor: Tl
	Save	Ctrl+S	Ĩ .
	Save As		
R	Save All	Ctrl+Shift+S	
	Revert		
	Move		
	Rename	F2	
8	Refresh	F5	
	Convert Line Delimiters To	÷.	
Ð	Print	Ctrl+P	
	Switch Workspace	•	D:\Linux\workspace
	Restart		Other

File->Switch Workspace->Other, select directory of the Lab example project.

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New create one project by click "NiosII Application and BSP from Template".







Select "SOPC", fill the "Project Name", and choose "Template" as "Simple Socket Server (RG...".

Nios II Application and BSP from Template		
Nios II Software Examples		
Please specify a .sopcinfo file		
Target hardware information		
SOPC Information File name:		
CPU name:	•	
Application project		
Project name:		
I lise default location		
Project location:		
Project template		
Templates Template description		
Hello MicroC/OS-II A Simple Socket Server uses Hello World Socket interface to TCP/	s the industry standard	<u>^</u>
Hello World Small how to initialize the Niche	Stack TCP/IP Stack and run a	=
Memory Test simple TCP server applica	tion, allowing a PC to	
Simple Socket Server	li system via Ethernet.	
Simple Socket Server (RG This example requires the	MicroC/OS-II RTOS and	
Web Server (RGMII) NicheStack TCP/IP Stack - components, It also requi	Nios II Edition software res several peripherals.	
including a lan91c111 Ethe	ernet MAC.	Ŧ
	t > Einich	Cancel
S Dack Nex		Cancer

打开	des .		×	
Work (I	D:) + Examples + NIOS_demo + -	搜索 NIOS_a	lemo 👂	
组织 ▼ 新建文件夹			:= • 🔟 🔞	
▲ ☆ 收藏夹	名称	修改日期	类型	
🗘 Dropbox	퉬 .metadata	2012/9/3 14:35	文件夹	
▶ 下载	📔 .qsys_edit	2012/9/3 14:35	文件夹	
三 桌面	🌗 db	2012/9/3 15:47	文件夹	
1 最近访问的位置	퉬 flash	2012/9/3 14:35	文件夹	
PDproject	FULL_SYS	2012/9/3 14:35	文件夹	
	퉬 greybox_tmp	2012/9/3 14:35	文件夹	
. <u>-</u> ≠	퉬 incremental_db	2012/9/3 14:35	文件夹	
	퉬 script	2012/9/3 14:35	文件夹	
	퉬 software	2012/9/3 14:53	文件夹	
🛛 🛃 视频	FULL_SYS.sopcinfo	2012/9/2 21:14	SOPCINFO 文件	
◎ 🔛 图片				
▶ 🖹 文档	•		-	
文件名(N): SOPC Information File (*.sop ▼				
		打开(O)	取消	





Modify file "simple_socket_server.h" as below.

```
h simple_socket_server.h 🛛
   * these values are only a valid default on networks with DHCP : .
   * If DHCP will not be used, select valid static IP addresses he
             IP: 192.168.1.234
         Gateway: 192.168.1.1
      Subnet Mask: 255.255.255.0
   */
  #define IPADDR0
                    0
  #define IPADDR1
                    0
  #define IPADDR2
                    0
  #define IPADDR3
                    0
  #define GWADDR0
                    0
  #define GWADDR1
                    0
  #define GWADDR2
                    0
  #define GWADDR3
                   0
  •
               ....
```

```
- -
h simple_socket_server.h 🛛 🗎
   * these values are only a valid default on networks with DHCP : \checkmark
   * If DHCP will not be used, select valid static IP addresses h\varepsilon
              IP: 192.168.1.234
          Gateway: 192.168.1.1
   *
      Subnet Mask: 255.255.255.0
   */
  #define IPADDR0
                     192
  #define IPADDR1
                     168
  #define IPADDR2
                     1
  #define IPADDR3
                     234
  #define GWADDR0
                     192
  #define GWADDR1
                     168
  #define GWADDR2
                     1
  #define GWADDR3 1
  Ш
```

Open network_utilities.c, search "ser_num = get_serial_number()" and replace it using "ser_num = 123456789" as below.

```
Inetwork_utilities.c ☎
h simple_socket_server.h
      printf("Can't read the MAC address from your board (this pro-
      printf("that your flash was erased). We will assign you a MJ
      printf("static network settings\n\n");
     //ser num = get serial number();
      ser num = 123456789;
                                                                    if (ser_num)
      {
          /* This says the image is safe */
          flash_content[0] = 0xfe;
          flash content[1] = 0x5a;
          flash content[2] = 0x0;
          flash_content[3] = 0x0;
   •
                                                                  Þ
                          III
```





Right click on the project, and select NiosII->BSP Editor.

Team Compare With Restore from Local History	+ +	080 080 080	30000 (58%) 40000 (77%) 50000 (97%)
Nios II	۰.		BSP Editor
Update Linked Resources			Nios II Command Shell
Properties	Alt+Enter	_	Flash Programmer

Click "Software Packages" label, remove "enable_dhcp_client" option. Then click "Generate".

Nios II BSP Editor - D:\Examples\NIOS_demo\so	ftware\demo2_bs	p\settings.bsp				
File Edit Tools Help						
Main Software Packages Drivers Linker Script Enable F	ile Generation Targ	et BSP Directory				
Software Package Name		Version	Enable			
altera_hostfs		default				
altera_iniche		default				
altera_quad_seven_seg		default				
altera_ro_zipfs		default				
	ble_dhcp_clieni ble_include_tcp ble_ip_fragments ble_net_stats ble_tcp_zerocopy default_if: r_USED					
Information Problems Processing						
Mapped module: "sys_timer" to use the default driver ver	sion.					
Mapped module: "led_pio" to use the default driver version	m.					
Mapped module: "button_pio" to use the default driver very set to use the default d	ersion.					
Mapped module: "jtag_uart" to use the default driver ver	sion.					
Mapped module: "ext_flash" to use the default driver ver	(i) Mapped module: "ext_flash" to use the default driver version.					
Finished loading drivers from ensemble report.						
Loading BSP settings from settings file.						
Finished loading SOPC Builder system info file "D: \Example	es\NIOS_demo\FULL_	_SYS.sopcinfo"				
Setting "altera_iniche.enable_dhcp_client" set to "false".					-	
				Generate	Exit	

There're 2 files under this directory, copy .h file to "demo2_bsp ->drivers->inc", and copy .c file to "demo2_bsp ->drivers->src", replace the original files.

rk (D:) ▶ Examples ▶ NIOS_demo ▶ softwa	re ▶		
共享 ▼ 新建文件夹			
名称	修改日期	类型	大小
퉬 demo2	2012/9/3 16:17	文件夹	
퉬 demo2_bsp	2012/9/3 16:16	文件夹	
📄 altera_avalon_tse.c	2012/6/12 17:28	UltraEdit Docum	104 KB
📄 altera_avalon_tse.h	2012/8/13 15:28	UltraEdit Docum	44 KB

ATERA.

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rk (D:) 🕨	Examples	۶.	NIOS_demo	۲	software	۲	demo2_bsp	►	drivers	۲	inc	۶.
-----------	----------	----	-----------	---	----------	---	-----------	---	---------	---	-----	----

+享 ▼ 新建文件夹

名称	修改日期	类型	大小
퉬 iniche	2012/9/3 16:09	文件夹	
📄 altera_avalon_cfi_flash.h	2012/9/3 16:09	UltraEdit Docum	9 KB
📄 altera_avalon_cfi_flash_amd_funcs.h	2012/9/3 16:09	UltraEdit Docum	4 KB
📄 altera_avalon_cfi_flash_funcs.h	2012/9/3 16:09	UltraEdit Docum	4 KB
📄 altera_avalon_cfi_flash_intel_funcs.h	2012/9/3 16:09	UltraEdit Docum	4 KB
📄 altera_avalon_epcs_flash_controller.h	2012/9/3 16:09	UltraEdit Docum	8 KB
📄 altera_avalon_jtag_uart.h	2012/9/3 16:09	UltraEdit Docum	8 KB
📄 altera_avalon_jtag_uart_fd.h	2012/9/3 16:09	UltraEdit Docum	6 KB
📄 altera_avalon_jtag_uart_regs.h	2012/9/3 16:09	UltraEdit Docum	5 KB
altera_avalon_pio_regs.h	2012/9/3 16:09	UltraEdit Docum	5 KB
📄 altera_avalon_sgdma.h	2012/9/3 16:09	UltraEdit Docum	10 KB
📄 altera_avalon_sgdma_descriptor.h	2012/9/3 16:09	UltraEdit Docum	6 KB
📄 altera_avalon_sgdma_regs.h	2012/9/3 16:09	UltraEdit Docum	7 KB
📄 altera_avalon_spi.h	2012/9/3 16:09	UltraEdit Docum	4 KB
📄 altera_avalon_spi_regs.h	2012/9/3 16:09	UltraEdit Docum	6 KB
📄 altera_avalon_timer.h	2012/9/3 16:09	UltraEdit Docum	10 KB
📄 altera_avalon_timer_regs.h	2012/9/3 16:09	UltraEdit Docum	11 KB
📄 altera_avalon_tse_system_info.h	2012/9/3 16:09	UltraEdit Docum	17 KB
epcs_commands.h	2012/9/3 16:09	UltraEdit Docum	1 KB
triple_speed_ethernet.h	2012/9/3 16:09	UltraEdit Docum	3 KB
triple_speed_ethernet_regs.h	2012/9/3 16:09	UltraEdit Docum	33 KB
📄 altera_avalon_tse.h	2012/8/13 15:28	UltraEdit Docum	44 KB

rk (D:) + Examples + NIOS_demo + software + demo2_bsp + drivers + src +

享▼ 新建文件夹			
名称	修改日期	建型	大小
🕌 iniche	2012/9/3 16:09	文件夹	
altera_avalon_cfi_flash.c	2012/9/3 16:09	UltraEdit Docum	12 KI
altera_avalon_cfi_flash_amd.c	2012/9/3 16:09	UltraEdit Docum	9 K
altera_avalon_cfi_flash_intel.c	2012/9/3 16:09	UltraEdit Docum	8 K
altera_avalon_cfi_flash_table.c	2012/9/3 16:09	UltraEdit Docum	19 K
altera_avalon_epcs_flash_controller.c	2012/9/3 16:09	UltraEdit Docum	15 K
altera_avalon_jtag_uart_fd.c	2012/9/3 16:09	UltraEdit Docum	4 K
altera_avalon_jtag_uart_init.c	2012/9/3 16:09	UltraEdit Docum	11 K
altera_avalon_jtag_uart_ioctl.c	2012/9/3 16:09	UltraEdit Docum	4 K
altera_avalon_jtag_uart_read.c	2012/9/3 16:09	UltraEdit Docum	7 K
altera_avalon_jtag_uart_write.c	2012/9/3 16:09	UltraEdit Docum	8 K
altera_avalon_sgdma.c	2012/9/3 16:09	UltraEdit Docum	30 K
altera_avalon_spi.c	2012/9/3 16:09	UltraEdit Docum	6 K
altera_avalon_timer_sc.c	2012/9/3 16:09	UltraEdit Docum	5 K
altera_avalon_timer_ts.c	2012/9/3 16:09	UltraEdit Docum	7 K
altera_avalon_timer_vars.c	2012/9/3 16:09	UltraEdit Docum	3 K
altera_avalon_tse.c	2012/6/12 17:28	UltraEdit Docum	104 K
altera_avalon_tse_system_info.c	2012/9/3 16:09	UltraEdit Docum	4 K
epcs_commands.c	2012/9/3 16:09	UltraEdit Docum	6 K





Build the project

Nios I	II - de	emo2/network_utilities.c - Eclipse	
File Ed		New	· · · · ·
📬 🗸		Go Into	
🖒 Proj		Open in New Window	2
4 📴 🤇	D	Сору	Ctrl+C
	Ē	Paste	Ctrl+V
	×	Delete	Delete
⊳	ð.	Remove from Context	Ctrl+Alt+Shift+Down
⊳		Move	
⊳		Rename	F2
	2	Import	
	4	Export	
⊳		Build Project	
		Clean Project	
	8	Refresh	F5
ניי		Close Project	
		Close Unrelated Projects	
		Build Configurations	+
		Make Targets	+
		Index	+
× ₩2		Convert To	1

Right click and select "Run As->NiosII Hardware"

 ▷ ▷ ○ ○	2 2	Import Export Build Project Clean Project Refresh Close Project Close Unrelated Projects Build Configurations Make Targets Index	F5	/* T flas flas flas flas flas tlas flas flas flas flas flas flas flas	his says the image is safe h_content[0] = 0xfe; h_content[1] = 0x5a; h_content[2] = 0x0; h_content[3] = 0x0; sks Console Properties Console Configuration - cable: USB-Blaster on localh ICP/IP, v3.1
		Run As	F		1 Lauterbach ISS
		Debug As	×	C	2 Local C/C++ Application
		Profile As	►	1/201	3 Nios II Hardware
		Team	•		4 Nios II ModelSim
		Compare With	•		Run Configurations
		Restore from Local History		_	Ū.



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Run "cmd", ping 192.168.1.234. Check if it can pass.



You can also use <u>PuTTY</u> to switch on/off LEDs on board. Launch PuTTY application, then configure it as below:

Basic options for your PuTTY sess becify the destination you want to connect ost Name (or IP address) 92.168.1.234 bonnection type: Raw Telnet Rlogin SSH bad, save or delete a stored session aved Sessions	ion to Port 30 © Serial
ecify the destination you want to connect ost Name (or IP address) 92.168.1.234 onnection type:) Raw Telnet Rlogin SSH oad, save or delete a stored session aved Sessions	to Port 30 © Serial
onnection type:) Raw Telnet Rlogin SSH bad, save or delete a stored session aved Sessions	⊚ Serial
aad, save or delete a stored session aved Sessions Default Settings	
Default Settings	
TemSession x11	Load Save Delete
ose window on exit:) Always 💿 Never 💿 Only on clea	an exit
	ose window on exit:) Always Never ⊚ Only on clea





Click "Open", then input a number range (0~3) to control D8, D7, D6, D9.



Reference capture of LED lights:







4.3 Lab 3

4.3.1 Objective

The following lab exercise is to demonstrate Cyclone IV GX PCIe hard IP and device data throughput performance. This design is based on Altera PCIe High Performance Reference Design (AN456)

4.3.2 Step by step

Install driver. Run install.bat.

ork (D:)	1 ▶ JungoDrivers		
新建文件夹			
名称	修改日期	类型	大小
altpcie_perf_demo_e001.inf	2036/2/5 6:28	安装信息	5 KB
🚳 install.bat	2012/9/3 14:44	Windows 批处理	1 KB
🚳 wdapi810.dll	2006/8/24 9:43	应用程序扩展	100 KB
💷 wdreg.exe	2006/6/6 6:44	应用程序	133 KB
indrvr6.inf	2006/8/15 4:33	安装信息	3 KB
🚳 windrvr6.sys	2006/8/15 4:32	系统文件	190 KB

If succeeded, you can see below ...







Download "top.sof" into the main board

Examples/PCIe_c4gx	_demo/top - top - [to	p.cdf]*						23
USB-Blaster [USB-0]	dow Help 🕏	Mode: JTAG		 Progres 	s:	100% (S	uccessful)	
File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check	Examine	Sec E
top.sof	EP4CGX22CF19	006AF7FA	FFFFFFF					
<		III						•
								* III +
	Examples/PCIe_c4gx	Examples/PCIe_c4gx_demo/top - top - [to cessing Tools Window Help USB-Blaster [USB-0] to allow background programming (for MAX II and File Device top.sof EP4CGX22CF19 TDI I I I I I I I I I I I I I I I I I I	Examples/PCIe_c4gx_demo/top - top - [top.cdf]* Decessing Tools Window Help USB-Blaster [USB-0] Mode: JTAG to allow background programming (for MAX II and MAX V devices) File Device Checksum top.sof EP4CGX22CF 19 006AF7FA	Examples/PCIe_c4gx_demo/top - top - [top.cdf]* Decessing Tools Window Help USB-Blaster [USB-0] Mode: JTAG to allow background programming (for MAX II and MAX V devices) File Device Checksum Usercode top.sof EP4CGX22CF19 006AF7FA FFFFFFFF TDI	Examples/PCIe_c4gx_demo/top - top - [top.cdf]* Decessing Tools Window Help Progres USB-Blaster [USB-0] Mode: TAG Progres to allow background programming (for MAX II and MAX V devices) File Device Checksum Usercode Program/ Configure top.sof EP4CGX22CF19 006AF7FA FFFFFFFF	Examples/PCIe_c4gx_demo/top - top - [top.cdf]*	Examples/PCIe_c4gx_demo/top - top - [top.cdf]*	Examples/PCIe_c4gx_demo/top - top - [top.cdf]*

Plug the main board into computer ExpressCard socket. If needed, please using the PCIe Expresscard adapter. After soft restart the computer, you can find the new device in the device list.







Double click the new PCI device

PCI Device 属性 ?区
常规 驱动程序 详细信息 资源
PCI Device
设备类型:其它设备
制造商:未知
位置: PCI Slot 6 (PCI 总线 3、设备 0、功能 0)
此设备的配置不正确。(代码 1)
要重新为这个设备安装驱动程序, 请单击"重新安装驱动程序"。
重新安装驱动程序 (I)
设备用法 (2):
使用这个设备(启用)
确定 取消

Click to reinstall the driver. Select "No...", then click "Next".







Select choose from manual directory as below and click "Next"



Select as below and click "Next"

硬件更新向导
请选择您的搜索和安装选项。
 在这些位置上搜索最佳驱动程序(S)。 使用下列的复选框限制或扩展默认搜索,包括本机路径和可移动媒体。会安装找 到的最佳驱动程序。
 ✓ 搜索可移动媒体(软盘、CD-ROM)(M) □ 在搜索中包括这个位置(Q): I:\ I:\
● 不要搜索。我要自己选择要安装的驱动程序 (D)。 选择这个选项以便从列表中选择设备驱动程序。Windows 不能保证您所选择的驱动程序与您的硬件最匹配。
< 上一步 (B) 下一步 (B) > 取消





Select "Jungo" from hardware type, then click "Next".

硬件更新向导	
硬件类型。	
选择一种硬件类型,然后单击"下一步"。	
常児硬件类型(J): ② IEEE 1394 IP 网络计数器 ③ IEEE 1394 和 SCSI 打印机 ③ IEEE 1394 急线主控制器 ③ Jungo 圖 Memory technology driver ③ NT Apm/Legacy 支持 圖 PCMCIA 卡 ③ SBP2 IEEE 1394 设备	
< 上一步 (B) 下一步 (B) > 取消	

Confirm "PCIe Performance Demo", click Next

硬件更新向导	
选择要为此硬件安装的设备驱动程序	
■ 諸选定硬件的厂商和型号,然后单击' Ⅰ 程序的磁盘,请单击"从磁盘安装"。	'下一步"。如果手头有包含要安装的驱动
型号 PCIe Performance Demo	
这个驱动程序没有经过数字签署! 告诉我为什么驱动程序签名很重要	从磁盘安装 (出)
	<上一步(26)下一步(26) > 取消





Select "Yes" for warning message.

更新驱	动程序警告 🛛 🕅
♪	不推荐安装这个驱动程序。原因是 Windows 无法确认这个驱动程序是否与硬件兼容。如果驱动程序不兼容,您的硬件将无法正常运行, 计算机可能会不稳定或完全停止正常运行。要继续安装这个驱动程序?
	是创一者创

Jungle PCIe driver will be installing.....

硬件更新向导				
向导正在3	安装软件,请稍候		E.	
E	PCIe Performance Demo			
	びたうした。 正在设置系统还原点 原系统。	。并备份旧文件,以防将来需要还		
		< 上一步 (B) 下一步 (B) >	取消	

Driver installed successfully.







Run the program below:

ork	(D:) ► Examples ► altpcie_demo_10.1 ►			
文件	浃			
	名称	修改日期	类型	大小
L]] JungoDrivers	2012/9/3 14:39	文件夹	
	🗊 altpcie_demo.exe	2010/11/8 9:35	应用程序	3,593 KB
	🚳 pci_lib.dll	2006/10/18 6:28	应用程序扩展	32 KB
	pcie_log.txt	2012/9/4 13:59	Text Document	69 KB
	🚳 wdapi810.dll	2006/8/24 9:43	应用程序扩展	100 KB
	🚳 wdapi811.dll	2006/10/18 6:29	应用程序扩展	100 KB

Run endpoint DMA

🎆 Altera Corporation - PCI Express - performance demo 🛛 🛛 🔀					
Cyclon	e IV GX		Performs	nce (MB/s)-	
Transfer length	100000				
Sequence:	Write only	_			
Number of			Peak	Average	Last
Doara:	Uyclone IV GX	- PC •	207	207	207
DMA write : 207 MB/s DMA write : 207 MB/s					
🦵 Continous loo			Run endpoir	nt DMA	





5 Appendix

AN 456: PCI Express High Performance Reference Design - Altera www.altera.com/literature/an/an456.pdf