DRAM Product Guide

1Q05

DRAM data sheets are available at ***www.micron.com/dramds***

DDR SDRAM - Double Data Rate (DDR) SDRAM

Density	Memory Configuration	Features	Part Number	Packages		Speed	Samples	Production
				TSOP (TG) Pins	FBGA Balls			
128Mb	32 Meg x 4	Quad-bank, 2.5V, SSTL_2	MT46V32M4	66	-	7.5	Now	Now
	32 Meg x 4	Quad-bank, 2.6V, SSTL_2	MT46V32M4	66	-	5	Now	Now
	16 Meg x 8	Quad-bank, 2.5V, SSTL_2	MT46V16M8	66	-	6, 7.5	Now	Now
	16 Meg x 8	Quad-bank, 2.6V, SSTL_2	MT46V16M8	66	-	5	Now	Now
	8 Meg x 16	Quad-bank, 2.5V, SSTL_2	MT46V8M16	66	-	7.5	Now	Now
	8 Meg x 16	Quad-bank, 2.6V, SSTL_2	MT46V8M16	66	-	5	Now	Now
256Mb	64 Meg x 4	Quad-bank, 2.5V, SSTL_2	MT46V64M4	66	60	6, 7.5	Now	Now
	64 Meg x 4	Quad-bank, 2.6V, SSTL_2	MT46V64M4	66	60	5	Now	Now
	32 Meg x 8	Quad-bank, 2.5V, SSTL_2	MT46V32M8	66	60	6, 7.5	Now	Now
	32 Meg x 8	Quad-bank, 2.6V, SSTL_2	MT46V32M8	66	60	5	Now	Now
	16 Meg x 16	Quad-bank, 2.5V, SSTL_2	MT46V16M16	66	60	6, 7.5	Now	Now
	16 Meg x 16	Quad-bank, 2.6V, SSTL_2	MT46V16M16	66	60	5	Now	Now
512Mb	128 Meg x 4	Quad-bank, 2.5V, SSTL_2	MT46V128M4	66	60	6, 7.5	Now	Now
	128 Meg x 4	Quad-bank, 2.6V, SSTL_2	MT46V128M4	66	60	5	Now	Now
	64 Meg x 8	Quad-bank, 2.5V, SSTL_2	MT46V64M8	66	60	6, 7.5	Now	Now
	64 Meg x 8	Quad-bank, 2.6V, SSTL_2	MT46V64M8	66	60	5	Now	Now
	32 Meg x 16	Quad-bank, 2.5V, SSTL_2	MT46V32M16	66	60	6, 7.5	Now	Now
	32 Meg x 16	Quad-bank, 2.6V, SSTL_2	MT46V32M16	66	60	5	Now	Now
1Gb	256 Meg x 4	Quad-bank, 2.5V, SSTL_2	MT46V256M4	66	-	6, 7.5	Now	Now
	64 Meg x 16	Quad-bank, 2.5V, SSTL_2	MT46V64M16	66	-	6, 7.5	Now	Now
	128 Meg x 8	Quad-bank, 2.5V, SSTL_2	MT46V128M8	66	-	6, 7.5	Now	Now

*DDR SDRAM is available in leaded or lead-free packages.

DDR2 SDRAM - Double Data Rate (DDR) SDRAM

Density	Memory Configuration	Features	Base Component Part Number	FBGA Balls	Speed Mark	Samples	Production
256Mb	64 Meg x 4	Quad-bank, 1.8V, SSTL_18	MT47H64M4BP	60	5E, 37E, 3	Now	Now
	32 Meg x 8	Quad-bank, 1.8V, SSTL_18	MT47H32M8BP	60	5E, 37E, 3	Now	Now
	16 Meg x 16	Quad-bank, 1.8V, SSTL_18	MT47H16M16BG	84	5E, 37E, 3	Now	Now
512Mb	128 Meg x 4	Quad-bank, 1.8V, SSTL_18	MT47H128M4BT	92	5E, 37E, 3	Now	Now
	128 Meg x 4	Quad-bank, 1.8V, SSTL_18	MT47H128M4CB	60	5E, 37E, 3	Now	1Q05
	64 Meg x 8	Quad-bank, 1.8V, SSTL_18	MT47H64M8BT	92	5E, 37E, 3	Now	Now
	64 Meg x 8	Quad-bank, 1.8V, SSTL_18	MT47H64M8CB	60	5E, 37E, 3	1Q05	2Q05
	32 Meg x 16	Quad-bank, 1.8V, SSTL_18	MT47H32M16BT	92	5E, 37E, 3	Now	Now
	32 Meg x 16	Quad-bank, 1.8V, SSTL_18	MT47H32M16CC	84	5E, 37E, 3	1Q05	2Q05
1Gb	256 Meg x 4	Eight-bank, 1.8V, SSTL_18	MT47H256M4BT	92	5E, 37E, 3	Now	Now
	128 Meg x 8	Eight-bank, 1.8V, SSTL_18	MT47H128M8BT	92	5E, 37E, 3	Now	Now
	64 Meg x 16	Eight-bank, 1.8V, SSTL_18	MT47H64M16BT	92	5E, 37E, 3	Now	1Q05

*DDR2 SDRAM is available in lead-free packages only.

(continued)

SDR SDRAM - Single Data Rate (SDR) SDRAM

Density	Memory Configuration	Features	Part Number	Packages		Speed Mark[1]	Samples	Production
				TSOP (TG) Pins	FBGA Balls			
64Mb	16 Meg x 4	Quad-bank, 3.3V	MT48LC16M4A2	54	-	7E, 7.5	Now	Now
	8 Meg x 8	Quad-bank, 3.3V	MT48LC8M8A2[2]	54	-	7E, 7.5	Now	Now
	4 Meg x 16	Quad-bank, 3.3V	MT48LC4M16A2[2, 3]	54	-	6, 7E, 7.5	Now	Now
	2 Meg x 32	Quad-bank, pipelined, 3.3V	MT48LC2M32B2[4]	86	-	5, 5.5, 6, 7	Now	Now
128Mb	32 Meg x 4	Quad-bank, 3.3V	MT48LC32M4A2	54	60	7E, 7.5	Now	Now
	16 Meg x 8	Quad-bank, 3.3V	MT48LC16M8A2[2]	54	60	7E, 7.5	Now	Now
	8 Meg x 16	Quad-bank, 3.3V	MT48LC8M16A2[2, 3]	54	-	6A, 7E, 7.5	Now	Now
	4 Meg x 32	Quad-bank, pipelined, 3.3V	MT48LC4M32B2[4]	86	90	6, 7	Now	Now
256Mb	64 Meg x 4	Quad-bank, 3.3V, 8K Refresh	MT48LC64M4A2	54	60	7E, 7.5	Now	Now
	32 Meg x 8	Quad-bank, 3.3V, 8K Refresh	MT48LC32M8A2[2]	54	60	6, 7E, 7.5	Now	Now
	16 Meg x 16	Quad-bank, 3.3V, 8K Refresh	MT48LC16M16A2[2, 3]	54	54	6, 7E, 7.5	Now	Now
	8 Meg x 32	Quad-bank, 3.3V, 4K Refresh	MT48LC8M32B2[4]	86	90	6, 7	Now	Now
512Mb	128 Meg x 4	Quad-bank, 3.3V, 8K Refresh	MT48LC128M4A2	54	-	7E, 7.5	Now	Now
	64 Meg x 8	Quad-bank, 3.3V, 8K Refresh	MT48LC64M8A2[2]	54	-	7E, 7.5	Now	Now
	32 Meg x 16	Quad-bank, 3.3V, 8K Refresh	MT48LC32M16A2[2]	54	-	7.5	Now	Now
	16 Meg x 32	Quad-bank, 3.3V, 4K Refresh	MT48LC16M32S2[4, 5]	-	90	6, 7	Now	1Q05

Note: *SDR SDRAM is available in leaded or lead-free packages. [1] -7 = PC133, CL = 2; -7.5 = PC133, CL = 3. [2]Available in industrial temp -75 IT or low-power self refresh -75L. [3]Available in industrial temp, -7E IT. [4]Available in industrial temp, -7 IT. [5]TwinDie™ solution.

Mobile DDR SDRAM (Low Power)

Density	Memory Configuration	Features[6]	Part Number[7]	FBGA Balls	Speed Mark	Samples	Production
128Mb	8 Meg x 16	PASR, TCSR, 1.8V	MT46H8M16LF	60	-75, -10	1Q05	2Q05
256Mb	16 Meg x 16	PASR, TCSR, DPD, 1.8V	MT46H16M16LF	60	-6, -7.5, -10	3Q05	1Q06
	8 Meg x 32	PASR, TCSR, DPD, 1.8V	MT46H8M32LF	90	-6, -7.5, -10	3Q05	1Q06
512Mb	32 Meg x 16	PASR, TCSR, DPD, 1.8V	MT46H32M16LF	60	-6, -7.5, -10	3Q05	1Q06
	16 Meg x 32	PASR, TCSR, DPD, 1.8V	MT46H16M32LF	90	-6, -7.5, -10	3Q05	1Q06

Note: [6]All parts have special low-power features and low VDDQ available for added power savings. [7]Available in industrial temperature (IT) range.
*Mobile DDR SDRAM is available in leaded or lead-free packages.

Mobile SDR SDRAM (Low Power)

Density	Memory Configuration	Features[6]	Part Number[7]	FBGA Balls	Speed Mark	Samples	Production
64Mb	4 Meg x 16	PASR, TCSR, DPD, 1.8V	MT48H4M16LF	54	-8, -10	Now	Now
128Mb	8 Meg x 16	PASR, TCSR, 3.3V	MT48LC8M16LF	54	-75, -8, -10	Now	Now
	8 Meg x 16	PASR, TCSR, 2.5V	MT48V8M16LF	54	-75, -8, -10	Now	Now
	8 Meg x 16	PASR, TCSR, DPD, 1.8V	MT48H8M16LF	54	-8, -10	Now	Now
	4 Meg x 32	PASR, TCSR, 2.5V	MT48V4M32LF	90	-75, -8, -10	Now	Now
	4 Meg x 32	PASR, TCSR, 3.3V	MT48LC4M32LF	90	-75, -8, -10	Now	Now
256Mb	16 Meg x 16	PASR, TCSR, DPD, 1.8V	MT48H16M16LF	54	-75, -8, -10	4Q05	2Q06
	8 Meg x 32	PASR, TCSR, DPD, 3.3V	MT48LC8M32LF	90	-75, -8, -10	Now	4Q04
	8 Meg x 32	PASR, TCSR, DPD, 2.5V	MT48V8M32LF	90	-75, -8, -10	Now	4Q04
	8 Meg x 32	PASR, TCSR, DPD, 1.8V	MT48H8M32LF	90	-75, -8, -10	Now	4Q04
512Mb	32 Meg x 16	PASR, TCSR, DPD, 1.8V	MT48H32M16LF	54	-75, -8, -10	4Q05	2Q06
	16 Meg x 32	PASR, TCSR, DPD, 1.8V	MT48H16M32LF	90	-75, -8, -10	4Q05	2Q06
	16 Meg x 32	PASR, TCSR, DPD, 3.3V	MT48LC16M32L2[8]	90	-8, -10	Now	1Q05
	16 Meg x 32	PASR, TCSR, DPD, 2.5V	MT48V16M32L2[8]	90	-8, -10	Now	1Q05
	16 Meg x 32	PASR, TCSR, DPD, 1.8V	MT48H16M32L2[8]	90	-8, -10	Now	1Q05

Note: [6]All parts have special low-power features and low VDDQ available for added power savings. [7]Available in industrial temperature (IT) range. [8]TwinDie solution.
*Mobile SDR SDRAM is available in leaded or lead-free packages.

(continued)

RLDRAM™ Memory[9]

Density	Memory Configuration	Description	Part Number	I/O Voltage	Package	Balls	Speed	Samples	Production
256Mb	16 Meg x 16	Eight-bank, 1.8V VDD, HSTL	MT49H16M16FM	1.8V	T-FBGA	144	3.3, 4. 5	Now	Now
	8 Meg x 32	Eight-bank, 1.8V VDD, HSTL	MT49H8M32FM	1.8V	T-FBGA	144	3.3, 4. 5	Now	Now

Note: [9]RLDRAM II devices are recommended for new designs.

RLDRAM II[9], Common I/O

Density	Memory Configuration	Description	Part Number	I/O Voltage	Package	Balls	Speed	Samples	Production
288Mb	32 Meg x 9	Eight-bank, 1.8V VDD, HSTL	MT49H32M9FM	1.5V / 1.8V	T-FBGA	144	2.5, 3.3, 5	Now	Now
	16 Meg x 18	Eight-bank, 1.8V VDD, HSTL	MT49H16M18FM	1.5V / 1.8V	T-FBGA	144	2.5, 3.3, 5	Now	Now
	8 Meg x 36	Eight-bank, 1.8V VDD, HSTL	MT49H8M36FM	1.5V / 1.8V	T-FBGA	144	2.5, 3.3, 5	Now	Now
576Mb	64 Meg x 9	Eight-bank, 1.8V VDD, HSTL	MT49H64M9FM	1.5V / 1.8V	T-FBGA	144	1.8, 2.5, 3.3, 5	2H06	2H06
	32 Meg x 18	Eight-bank, 1.8V VDD, HSTL	MT49H32M18FM	1.5V / 1.8V	T-FBGA	144	1.8, 2.5, 3.3, 5	2H06	2H06
	16 Meg x 36	Eight-bank, 1.8V VDD, HSTL	MT49H16M36FM	1.5V / 1.8V	T-FBGA	144	1.8, 2.5, 3.3, 5	2H06	2H06

RLDRAM II[9], Separate I/O

Density	Memory Configuration	Description	Part Number	I/O Voltage	Package	Balls	Speed	Samples	Production
288Mb	32 Meg x 9	Eight-bank, 1.8V VDD, HSTL	MT49H32M9CFM	1.5V / 1.8V	T-FBGA	144	2.5, 3.3, 5	Now	Now
	16 Meg x 18	Eight-bank, 1.8V VDD, HSTL	MT49H16M18CFM	1.5V / 1.8V	T-FBGA	144	2.5, 3.3, 5	Now	Now
576Mb	64 Meg x 9	Eight-bank, 1.8V VDD, HSTL	MT49H64M9CFM	1.5V / 1.8V	T-FBGA	144	1.8, 2.5, 3.3, 5	2H06	2H06
	32 Meg x 18	Eight-bank, 1.8V VDD, HSTL	MT49H32M18CFM	1.5V / 1.8V	T-FBGA	144	1.8, 2.5, 3.3, 5	2H06	2H06

Note: [9]RLDRAM II devices are recommended for new designs.

DRAM Component Part Numbering System

The part numbering system is available at ***www.micron.com/numberguide***

SDR/DDR/DDR2, Mobile SDRAM, and RLDRAM®

MT 48 LC 32M8 A2 TG - 7E L ES :D

Micron Technology

Product Family
46 = DDR SDRAM
47 = DDR2
48 = SDRAM/Mobile SDRAM
49 = RLDRAM

Process Technology
C = 5V VCC CMOS
G = 3.0V VDD CMOS
LC = 3.3V VDD CMOS
V = 2.5V VDD CMOS
H = 1.8V VDD CMOS
J = 1.5V VDD CMOS
N = 1.0V VDD CMOS

Device Number
Depth, Width
No Letter = Bits
K = Kilobits
M = Megabits
G = Gigabits

Device Versions
Alphanumeric character(s) specified by individual data sheet.
"LF" designates Mobile device.
"L2" and "S2" devices are made with dual die in package.

RLDRAM only
Blank = Common I/O
C = Separate I/O

Package Codes*

Die revision designator

Special Processing
ES = Engineering Sample
MS = Mechanical Sample
K = Interim Offering
H = Interim Offering
DM = Custom

Operating Temperatures
Blank = 0°C to +70°C
WT = -25°C to +85°C
IT** = -40°C to +85°C
XT = -25°C to +75°C
**The number one

Special Options
(Multiple processing codes are separated by a space and are listed in hierarchical order.)
L = Low Power

Access/Cycle Time

DRAM Technology	Speed Grade Mark	tRAC Access Time
All DRAM	-0	Untested
	-A	Untested

DRAM Technology	Speed Grade Mark	MAX Clock Frequency	PC Targets CL-tRCD-tRP
SDRAM	-75	133 MHz	3-3-3
	-7E	133 MHz	2-2-2
	-7	143 MHz	
	-6	167 MHz	
	-6A	167 MHz	
	-55	183 MHz	
	-5	200 MHz	
Mobile SDRAM	-10	100 MHz	2-2-2
	-8	125 MHz	2-2-2
	-75	133 MHz	3-3-3
Mobile DDR SDRAM	-10	100 MHz	
	-75	133 MHz	
DDR SDRAM	-75	133 MHz	2.5-3-3
	-75Z	133 MHz	2-3-3
	-75E	133 MHz	2-2-2
	-65	150 MHz	
	-6G	167 MHz	
	-6T	167 MHz	2.5-3-3
	-6R	167 MHz	2.5-3-3
	-6	167 MHz	2.5-3-3
	-55	183 MHz	
	-5T	200 MHz	3-4-4
	-5B	200 MHz	3-3-3
	-5A	200 MHz	2.5-3-3
	-5	200 MHz	
	-4	250 MHz	
	-33	300 MHz	
DDR2 SDRAM	-5	200 MHz	4-4-4
	-5E	200 MHz	3-3-3
	-37E	267 MHz	4-4-4
	-3	333 MHz	5-5-5
	-25	400 MHz	6-6-6
RLDRAM	-5	200 MHz	
	-4	250 MHz	
	-33	300 MHz	
	-25	400 MHz	
	-18	533 MHz	

Lead Plating	Pb-Free Plating	Package Description**
SDRAM		
FB	BB	FBGA (60-ball, 8 x 16)
FG	BG	VFBGA (54-ball); FBGA (84-ball, 60-ball, 8 x 14)
FJ	BJ	FBGA (60-ball, 9 x 16)
F4	B4	VFBGA (54-ball, 8 x 8)
F5	B5	VFBGA (90-ball, 8 x 13)
TG	P	TSOP (Type II)
xTG	xP	Stacked TSOP, "x" = internal stacking code
Mobile SDRAM		
F4	B4	VFBGA (54-ball, 8 x 8)
FF	BF	FBGA (54-ball, 8 x 9)
F5	B5	VFBGA (90-ball, 8 x 13)
FG	BG	FBGA (84-ball, 60-ball, 8 x 14)
	CJ	VFBGA (54-ball, 10 x 11.5)
	CM	VFBGA (90-ball, 10 x 12)
TG	P	TSOP (Type II)
xTG	xP	Stacked TSOP, "x" = internal stacking code
Mobile DDR SDRAM		
	CF	VFBGA (60-ball, 8 x 10)
	CK	VFBGA (60-ball, 10 x 11.5)
	CM	VFBGA (90-ball, 10 x 12)
DDR SDRAM		
FG	BG	FBGA (84-ball, 60-ball, 8 x 14)
FN	BN	FBGA (54-ball, 60-ball; 84-ball; 10 x 12.5)
TG	P	TSOP (Type II)
xTG	xP	Stacked TSOP, "x" = internal stacking code
DDR2 SDRAM		
	BP	FBGA (60-ball, 8 x 12)
	BG	FBGA (84-ball, 60-ball, 8 x 14)
	BT	FBGA (92-ball; 11 x 19)
	CB	FBGA (60-ball, 12 x 10)
	CC	FBGA (84-ball, 12 x 12.5)
RLDRAM		
FM	BM	FBGA (144-ball; 11 x 18.5)

*Due to space limitations, FBGA- and µBGA-packaged components and flip chips in packages have an abbreviated part mark that is different from the part number. See our Web site for more information on abbreviated component marks.

**Dimensions in millimeters

Some device offerings are available in a VFBGA rather than an FBGA package; this is noted on the data sheet.

Rev. 01-12-05

Pb-Free DRAM Component Part Numbering System

The part numbering system is available at ***www.micron.com/numberguide***

SDR/DDR/DDR2, Mobile SDRAM, and RLDRAM®

MT 48 LC 32M8 A2 P - 7E L ES :D

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Depth, Width
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RLDRAM only
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MS = Mechanical Sample
K = Interim Offering
H = Interim Offering
DM = Custom

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Blank = 0°C to +70°C
WT = -25°C to +85°C
IT** = -40°C to +85°C
XT = -25°C to +75°C
**The number one (1) and the capital letter "I" utilize the same laser mark—"I."

Special Options
(Multiple processing codes are separated by a space and are listed in hierarchical order.)
L = Low Power

Access/Cycle Time

DRAM Technology	Speed Grade Mark	^{t}RAC Access Time
All DRAM	-0	Untested
	-A	Untested

Pb-Free Plating	Package Description**
SDRAM	
BB	FBGA (60-ball, 8 x 16)
BG	VFBGA (54-ball); FBGA (84-ball, 60-ball, 8 x 14)
B4	VFBGA (54-ball, 8 x 8)
B5	VFBGA (90-ball, 8 x 13)
P	TSOP (Type II)
xP	Stacked TSOP, "x" = internal stacking code
Mobile SDRAM	
B4	VFBGA (54-ball, 8 x 8)
BF	FBGA (54-ball, 8 x 9)
B5	VFBGA (90-ball, 8 x 13)
BG	FBGA (84-ball, 60-ball, 8 x 14)
CJ	VFBGA (54-ball, 10 x 11.5)
CM	VFBGA (90-ball, 10 x 12)
P	TSOP (Type II)
xP	Stacked TSOP, "x" = internal stacking code
Mobile DDR SDRAM	
CF	VFBGA (60-ball, 8 x 10)
CK	VFBGA (60-ball, 10 x 11.5)
CM	VFBGA (90-ball, 10 x 12)
DDR SDRAM	
BG	FBGA (84-ball, 60-ball, 8 x 14)
BN	FBGA (54-ball, 60-ball; 84-ball; 10 x 12.5)
P	TSOP (Type II)
xP	Stacked TSOP, "x" = internal stacking code
DDR2 SDRAM	
BP	FBGA (60-ball, 8 x 12)
BG	FBGA (84-ball, 60-ball, 8 x 14)
BT	FBGA (92-ball; 11 x 19)
CB	FBGA (60-ball, 12 x 10)
CC	FBGA (84-ball, 12 x 12.5)
RLDRAM	
BM	FBGA (144-ball; 11 x 18.5)

DRAM Technology	Speed Grade Mark	MAX Clock Frequency	PC Targets CL-^{t}RCD-^{t}RP
SDRAM	-75	133 MHz	3-3-3
	-7E	133 MHz	2-2-2
	-7	143 MHz	
	-6	167 MHz	
	-6A	167 MHz	
	-55	183 MHz	
	-5	200 MHz	
Mobile SDRAM	-10	100 MHz	2-2-2
	-8	125 MHz	2-2-2
	-75	133 MHz	3-3-3
Mobile DDR SDRAM	-10	100 MHz	
	-75	133 MHz	
DDR SDRAM	-75	133 MHz	2.5-3-3
	-75Z	133 MHz	2-3-3
	-75E	133 MHz	2-2-2
	-65	150 MHz	
	-6G	167 MHz	
	-6T	167 MHz	2.5-3-3
	-6R	167 MHz	2.5-3-3
	-6	167 MHz	2.5-3-3
	-55	183 MHz	
	-5T	200 MHz	3-4-4
	-5B	200 MHz	3-3-3
	-5A	200 MHz	2.5-3-3
	-5	200 MHz	
	-4	250 MHz	
	-33	300 MHz	
DDR2	-5	200 MHz	4-4-4
	-5E	200 MHz	3-3-3
	-37E	267 MHz	4-4-4
	-3	333 MHz	5-5-5
	-25	400 MHz	6-6-6
RLDRAM	-5	200 MHz	
	-4	250 MHz	
	-33	300 MHz	
	-25	400 MHz	
	-18	533 MHz	

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