EasyGX

GX Development Kit Guide

Ver: 1.0

Cytech Technology
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Reversion History

Updated Date	Owner	Reversion	Updated Item
2012-10-29	John Lee	Draft 1.0	English edition
2012-02-14	MS	Draft 1.0	Content revised
2013-04-24	John Lee	Draft 1.0	File format adjustment
2013-04-25	John Lee	V1.0	English version released

Catelogue

1 Introduction

Thank you for your interest in the EasyGX Cyclone® IV GX Development Kit. This kit provides a general hardware platform for developing and prototyping low power, high volume, feature rich designs based on Cyclone® IV GX transceiver FPGA.

The EasyGX Cyclone® IV GX development kit is especially suitable for develop and test PCI Express and 10/100/1000M Ethernet interface, including NIOS II embedded CPU and USB-Blaster function, which provided rich external memory for rapid prototype environment.

1.1 Kit Contents

The EasyGX Cyclone® IV GX Development Kit basic package contains:

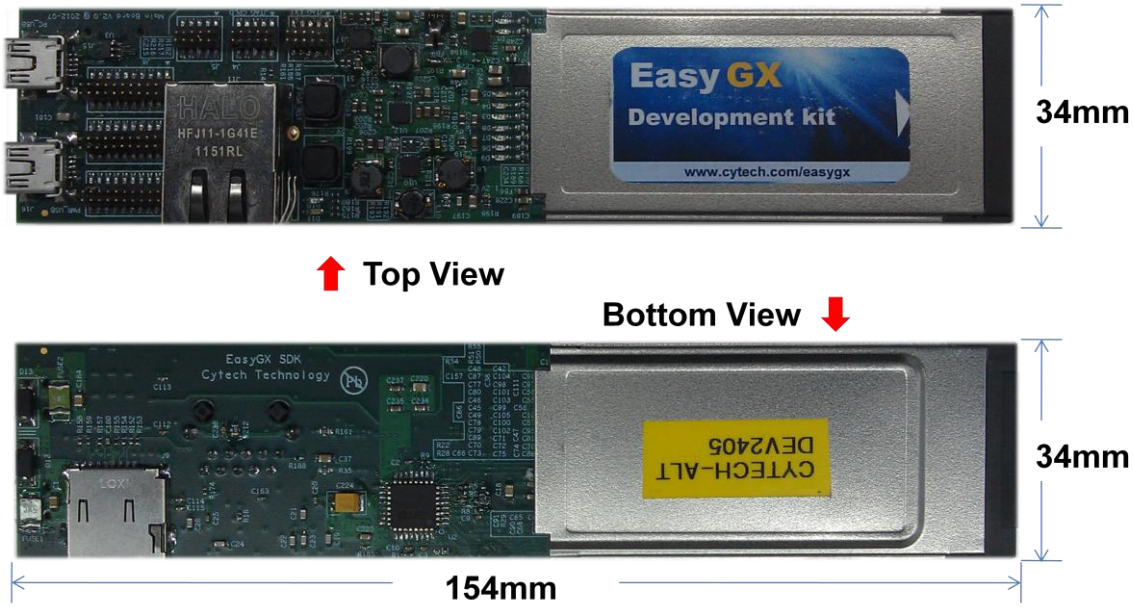
- Development main board
- USB Blaster expansion board with cable
- USB cable

Optional accessories (not included in basic package):

- PCI-e to 34mm ExpressCard 2.0 adapter
- Other function daughter boards will be released in the future

The picture below is shown for reference; See exact deliverable as standard.

Main board



1.2 Features

- Cyclone® IV GX EP4CGX22F324C8N FPGA in 324-pin FineLine BGA (FBGA) package
  - 21,280 LEs
  - 756kb embedded memory, 84 M9K blocks
  - 40 DSP blocks (18x18 bits)
  - PCI Express hard IP block
  - 1.2-V core voltage power
- MAX® V 5M80ZE64C5N CPLD in 64-pin plastic Enhanced quad flat pack (EQFP) package
  - 2.5-V core voltage power
- FPGA configuration circuitry
  - MAX V CPLD 5M80Z system controller
  - Embedded on-board USB-Blaster
  - JTAG-based header
  - Erasable programmable configurable serial (EPCS) device
- Transceiver interface
  - PCI Express v1.0 x1 ExpressCard interface
  - 10/100/1000BASE-T Ethernet PHY with RJ-45 connector
  - Two TX/RX transceiver SERDES loopback
- On-Board memeory
  - Micron DDR2 64Mx16 SDRAM MT47H64M16HR-25E:H
  - Altera 16Mb serial flash EPCS16S18N
- Power supply
  - 5V-dc USB input
  - 3.3V-dc PCIe ExpressCard
- Micro-SD card RW supported
- Altera Nios II embedded processor
- IDE base on Eclipse supported
- Include RTOS-Micrium uC/OS-II

1.3 Design Software

Type	Software	
Logic Design	QUARTUS II	ModelSim. Altera's version of ModelSim® Software
Embedded Design	Nios II	
DSP Design	DSP Builder	

Download linkage: http://www.altera.com/products/software/sfw-index.jsp

2 Getting Started

This chapter describes how to install and configure Altera Quartus II software environment

2.1 Software installation

2.1.1 Software introduction

Quartus II software includes everything you need to design Altera FPGA and CPLD families

2.1.1.1 About Quartus version

Web-edition and Subscription-edition is available for downloading via Altera official website. The following will be demonstrated based on Quartus II v12.0 version.

2.1.2 System requirements

2.1.2.1 Hardware requirements

- Windows PC or Linux work station
- Display resolution no less than 768*1024
- Enough hard disk space

2.1.2.2 Interface

- One UART
- USB Host
- 10/100M Ethernet

2.1.3 Installation

2.1.3.1 Download Quartus II software

You can download it from here. There're two methods：

1） Altera Installer

Using Altera Installer, you can download and install the Altera software for Windows or Linux. And you can choose necessary items

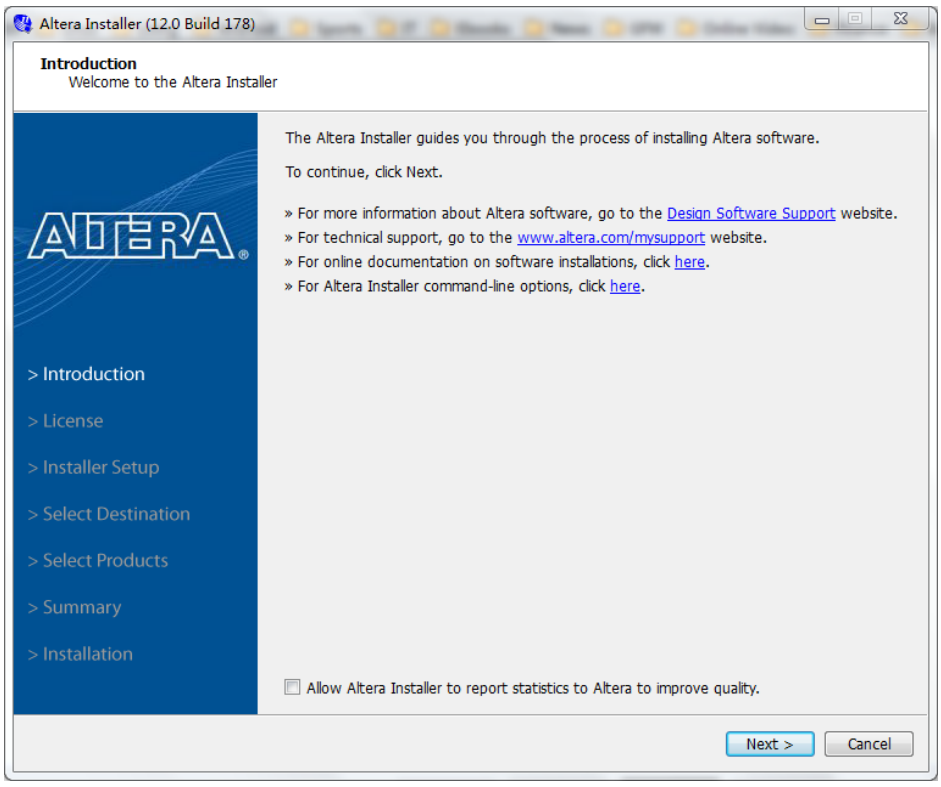
2） Individual software file

You can download some individual installation packages on the page. You can choose this method if clearly know about what items is needed

2.1.4 Install Quartus II

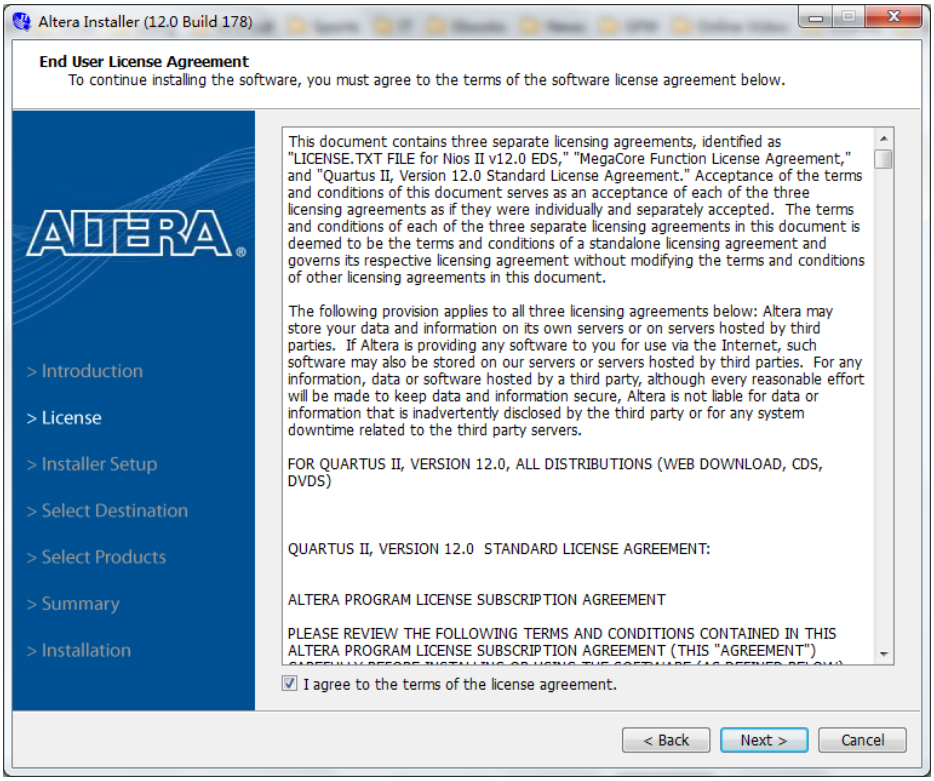
Procedure below is based on “Altera Installer”.

1） Launch “Altera Installer”.

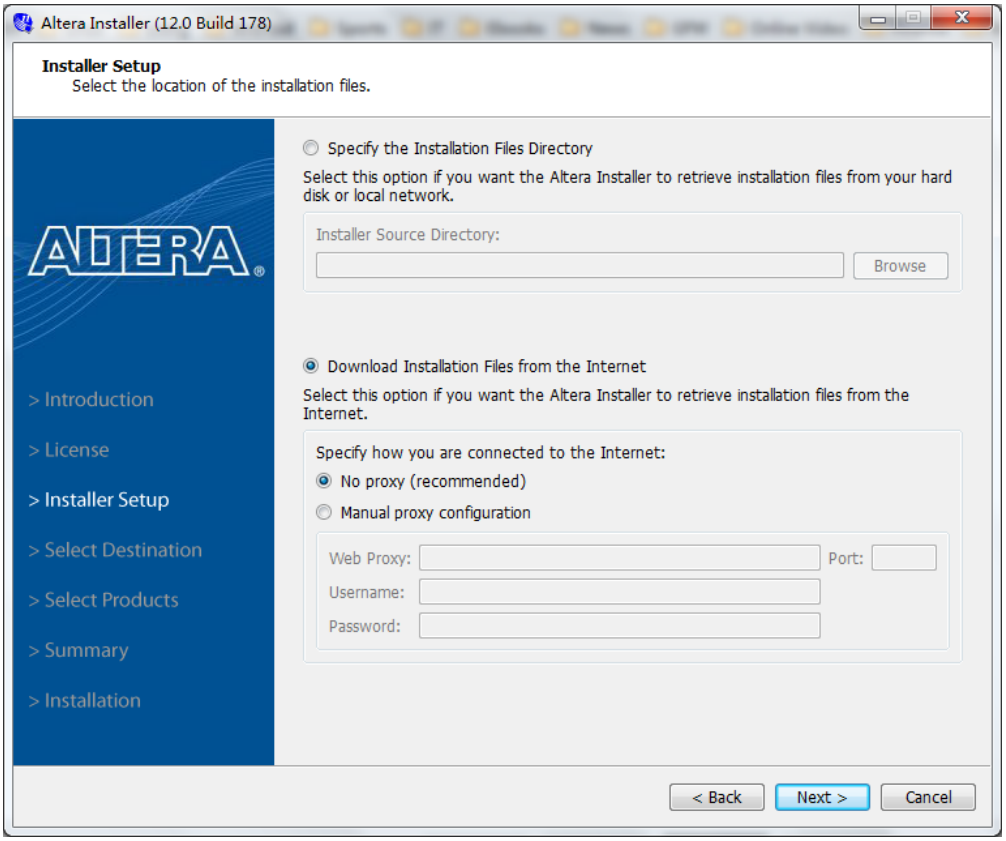


2） “Altera Installer” leads you to install…

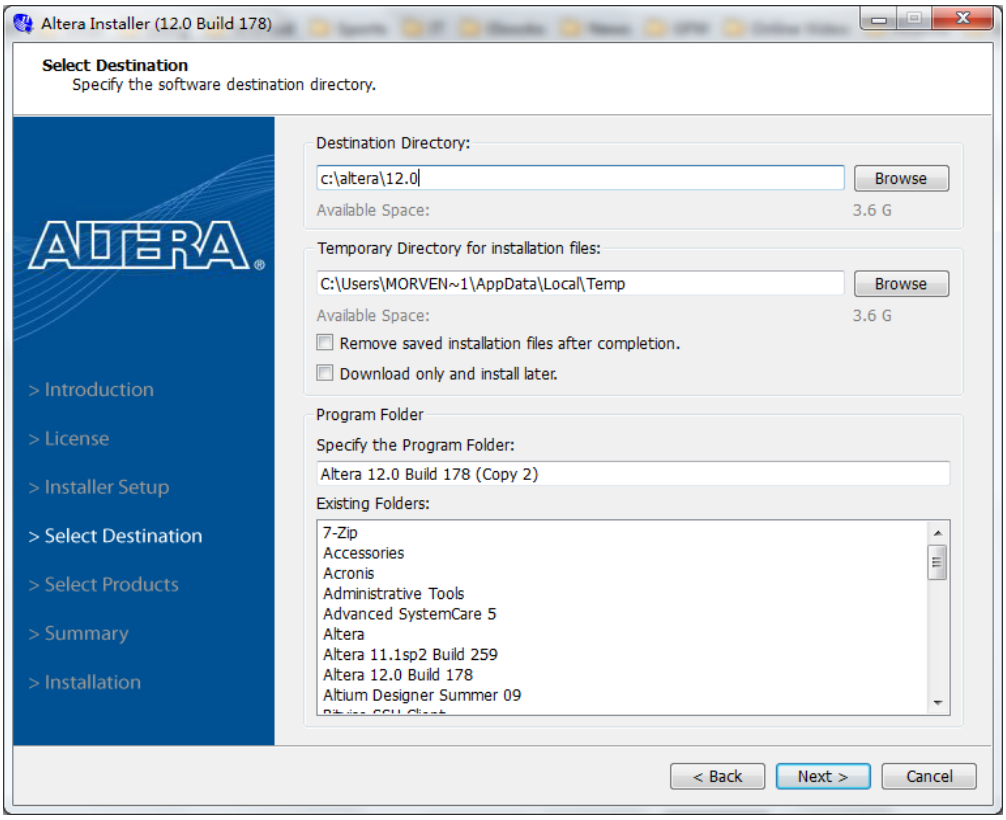
a) Agree and click “next” button.



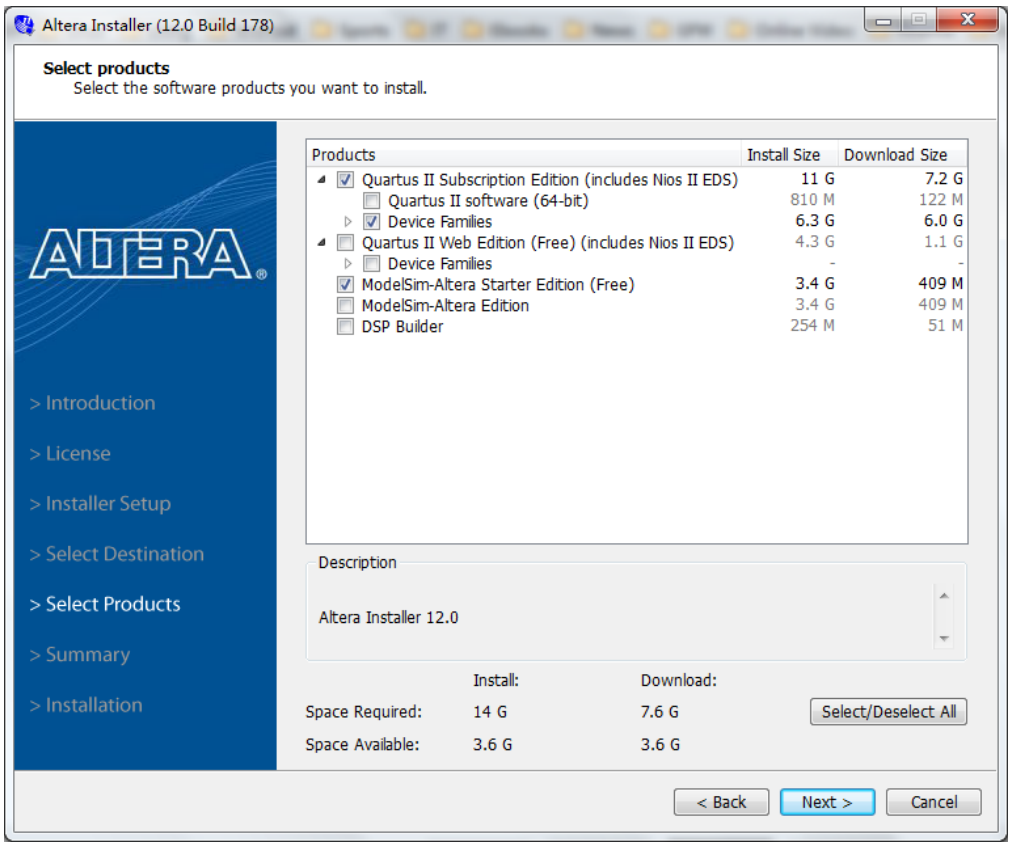
b) If you have not downloaded the installation package, please select as below.



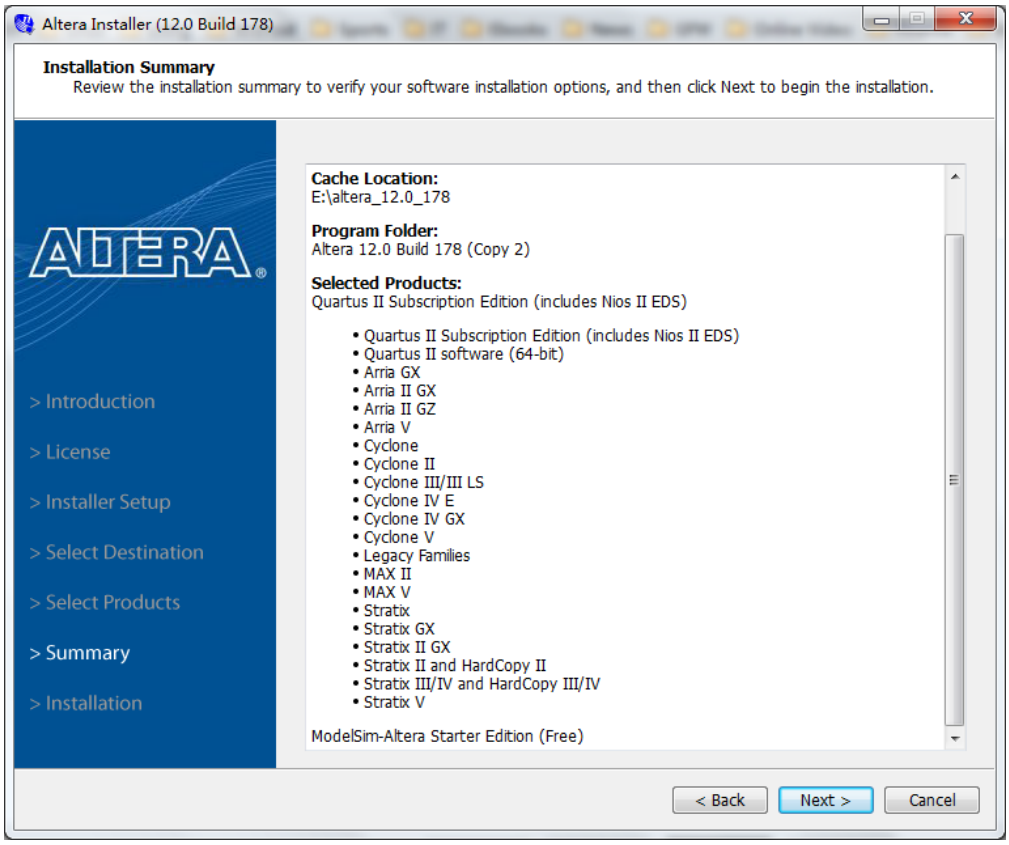
c) Choose the installation direction, and pay attention to the hard disk capacity.



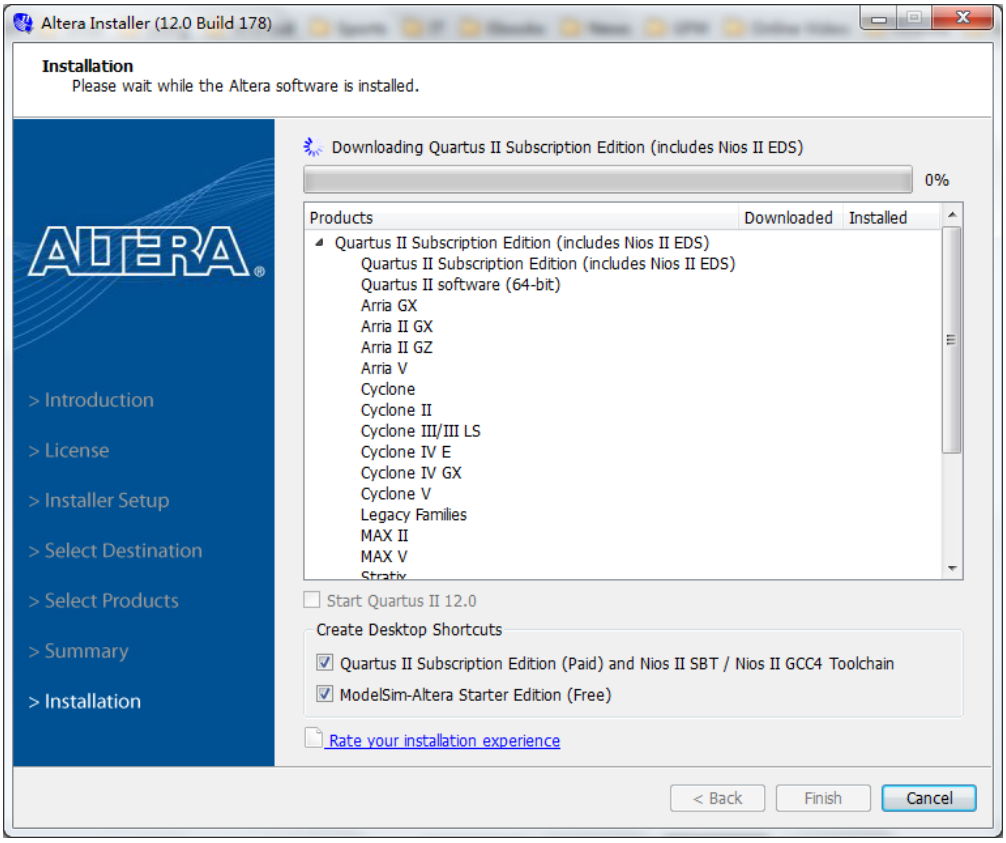
d) Select the devices and items needed.



e) Confirm Installation Summary, click Next.



f) Download and install.



2.1.5 Acquire license

If you choose free “Web” version, there’s no license needed; If you choose “Subscription” version，you need to acquire a license. About how to acquire and activate the license，please purchase subscription license from Altera or authorized distributor.

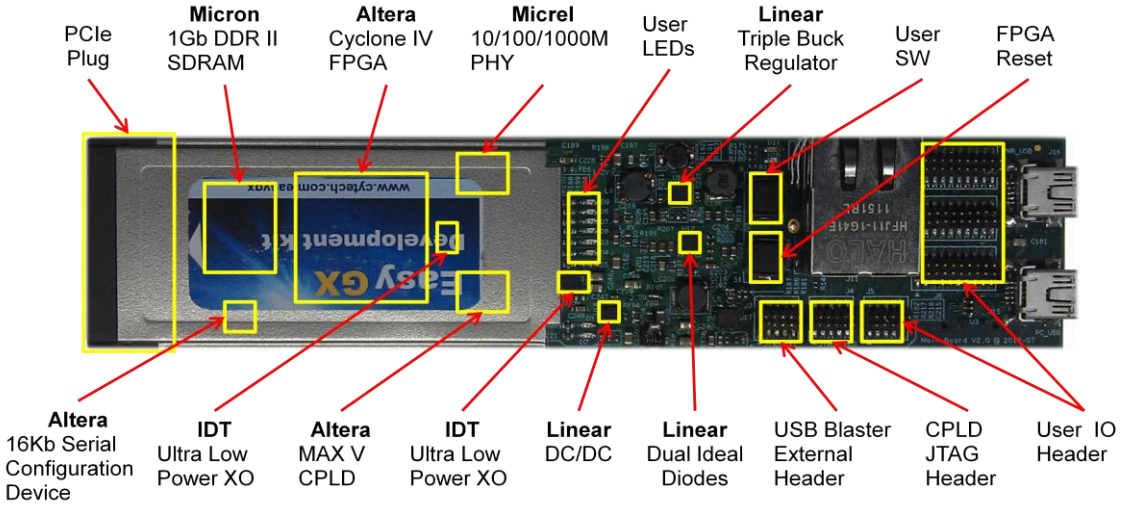
2.2 Hardware installation

There’s no hardware installation needed.

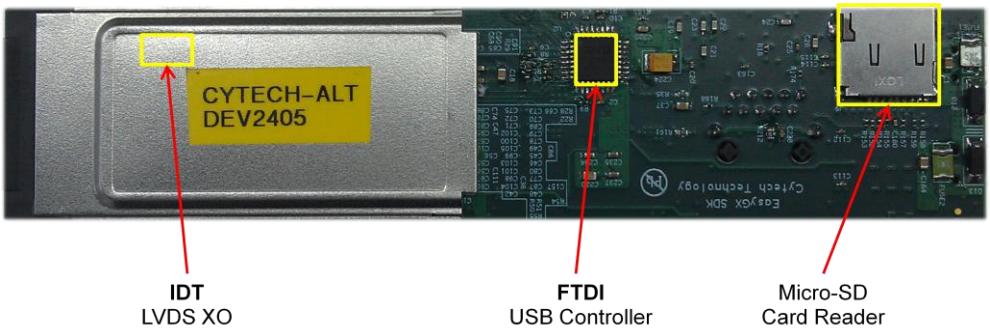
3 Hardware

3.1 Overview

3.1.1 Main board top view

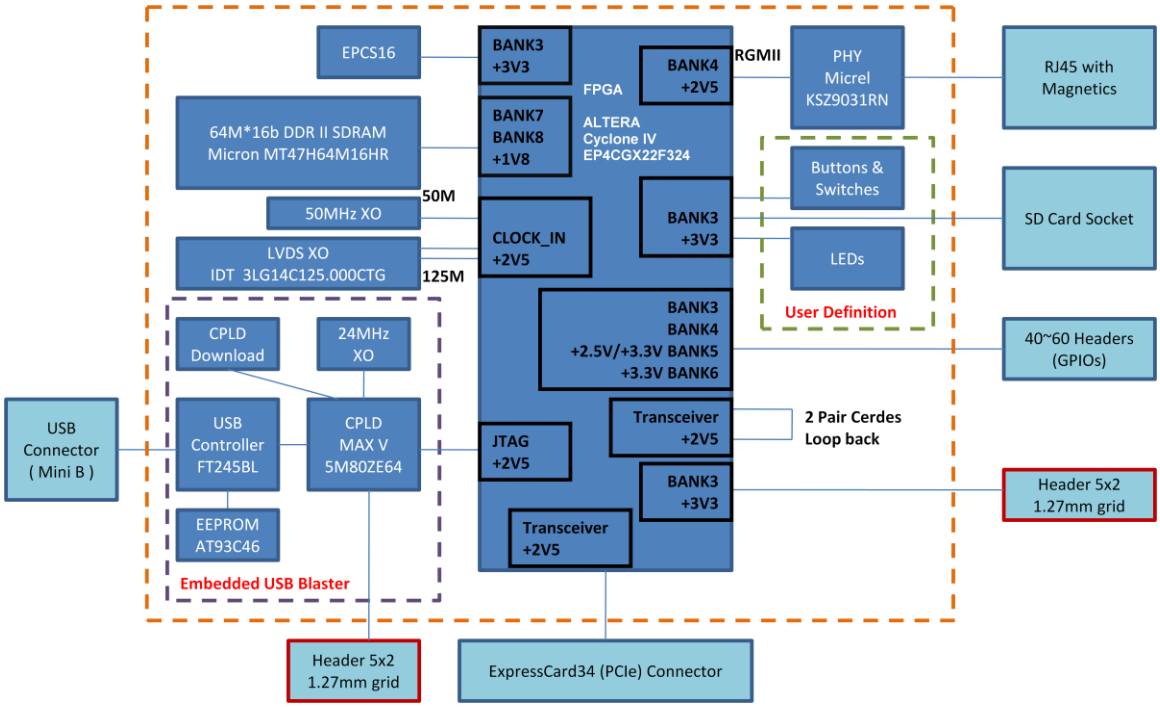


3.1.2 Main board bottom view

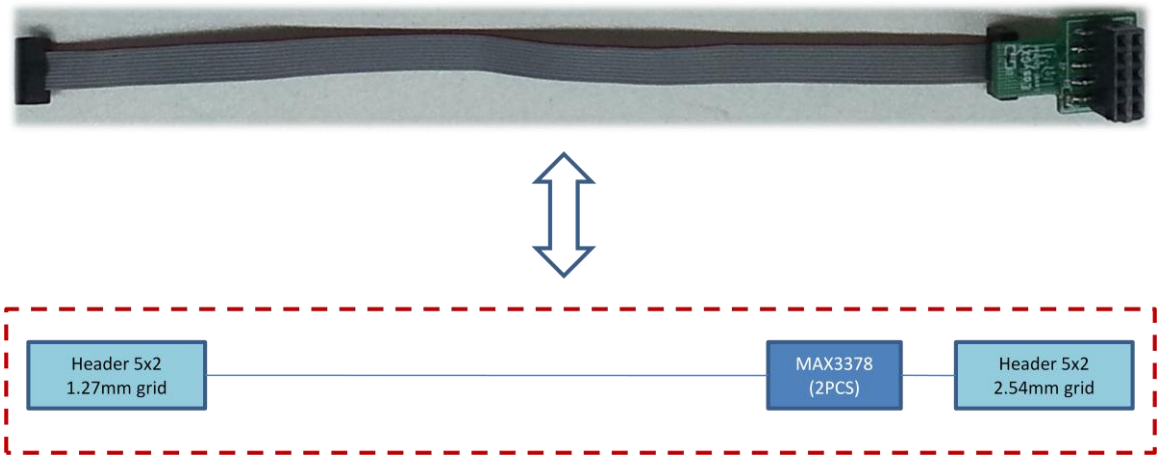


3.2 EasyGX hardware – Main board

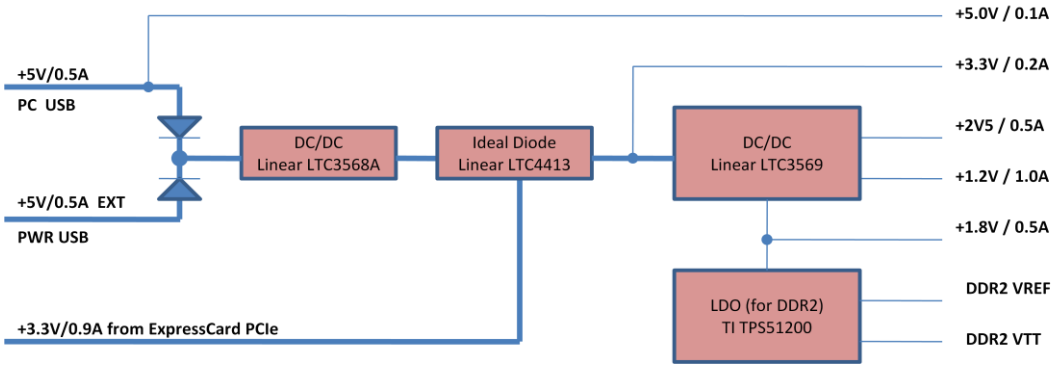
3.2.1 Main board system block diagram



3.2.2 USB Blaster expansion board diagram



3.2.3 Power supply chain



3.2.4 Function block introduction

3.2.4.1 Power configuration of FPGA

Cyclone ® IV GX power requirement:

Power pin	Voltage（V）	Comments
VCCINT	1.2	Core voltage、Power source of PCI Express (PCIe) hardcore IP module and transceiver physical coding sublayer (PCS)
VCCA	2.5	PLL analog power supply
VCCD_PLL	1.2	PLL digital power supply
VCCIO	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	I/O power supply
VCC_CLKIN	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	Power supply for differential clock input pin
VCCH_GXB	2.5	Power supply for Transceiver output (TX) buffer
VCCA_GXB	2.5	Power supply for transceiver physical media auxiliary sublayer (PMA) and auxiliary
VCCL_GXB	1.2	Power supply for transceiver PMA and auxiliary

1) Even if there's no PLL used, VCCA should be powered still.

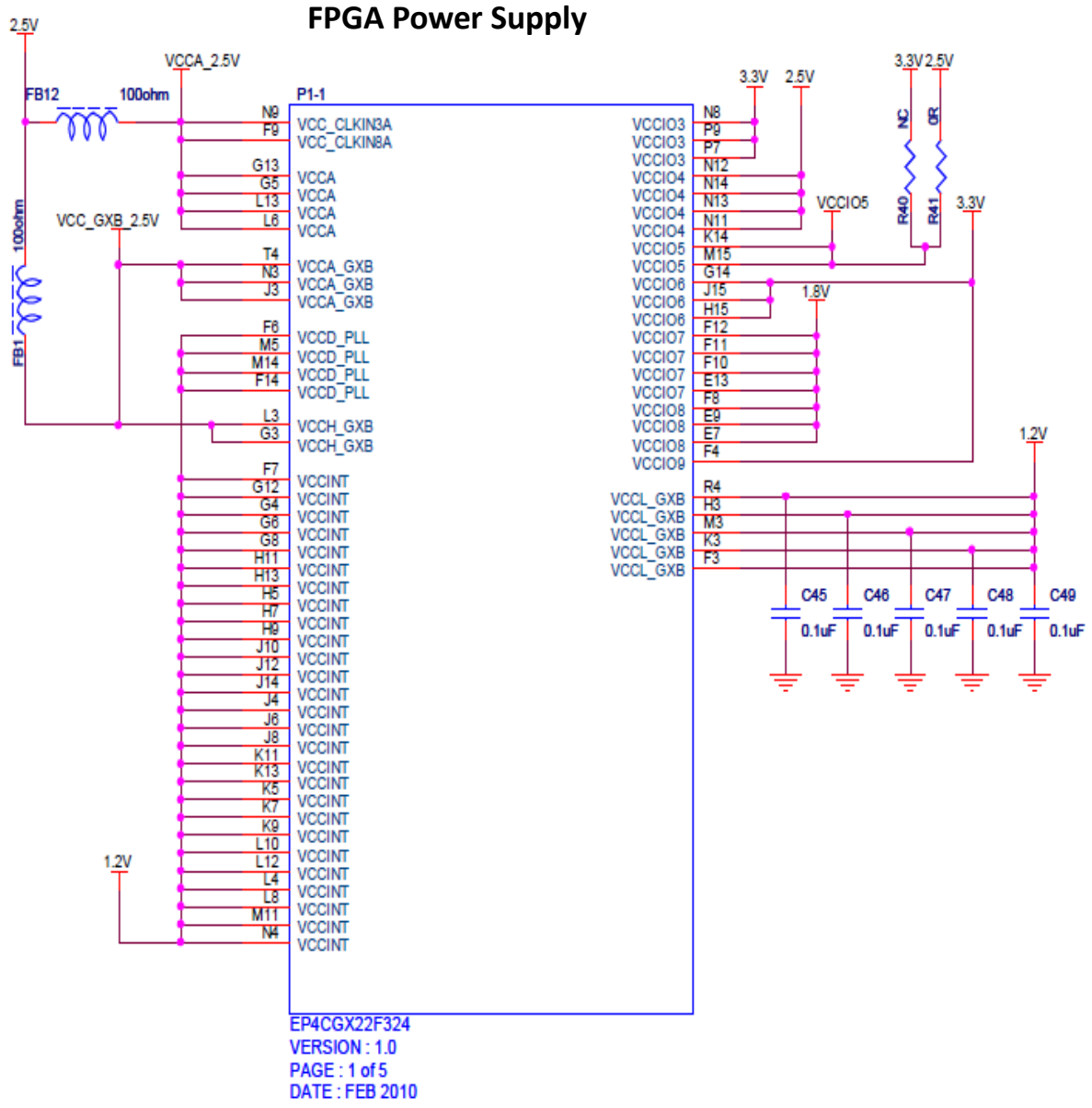
2) I/O bank 3、8 and 9 include configuration pins. You have to power I/O bank 3 and 9 VCCIO to 1.5 V、1.8 V、2.5 V、3.0 V or 3.3 V. As to FPP configuration mode, you should power I/O bank 8 VCCIO to 1.5 V、1.8 V、2.5 V、3.0 V or 3.3 V.

3) EP4CGX15、EP4CGX22 (in all package types) and EP4CGX30 (in package F169 and F324) have VCC_CLKIN I/O special for clock input locates on bank 3A and 8A. EP4CGX30 (in F484 package)、EP4CGX50、EP4CGX75、EP4CGX110 and EP4CGX150 (in all package types) have 4 VCC_CLKIN I/Os special for clock input locate on bank 3A、3B、8A and 8B.

4) If CLKIN is used as the refclk of high speed serial interface (HSSI), VCC_CLKIN should be set

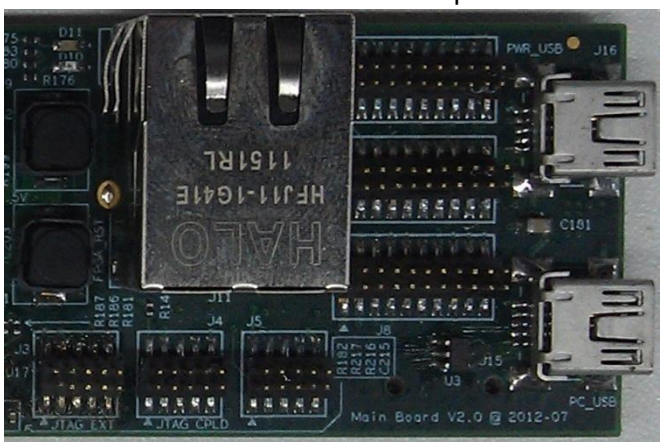
2.5V. VCC_CLKIN locates on I/O bank 3B and 8B must use 2.5V to support LVDS function, for they are dedicated pins for HSSI refclk. As to EP4CGX50、EP4CGX75、EP4CGX110 and EP4CGX150, single ended input CLK can be used as dedicated input CLK located on I/O bank 3B and 8B.

Power supply configuration schematic of FPGA as below:

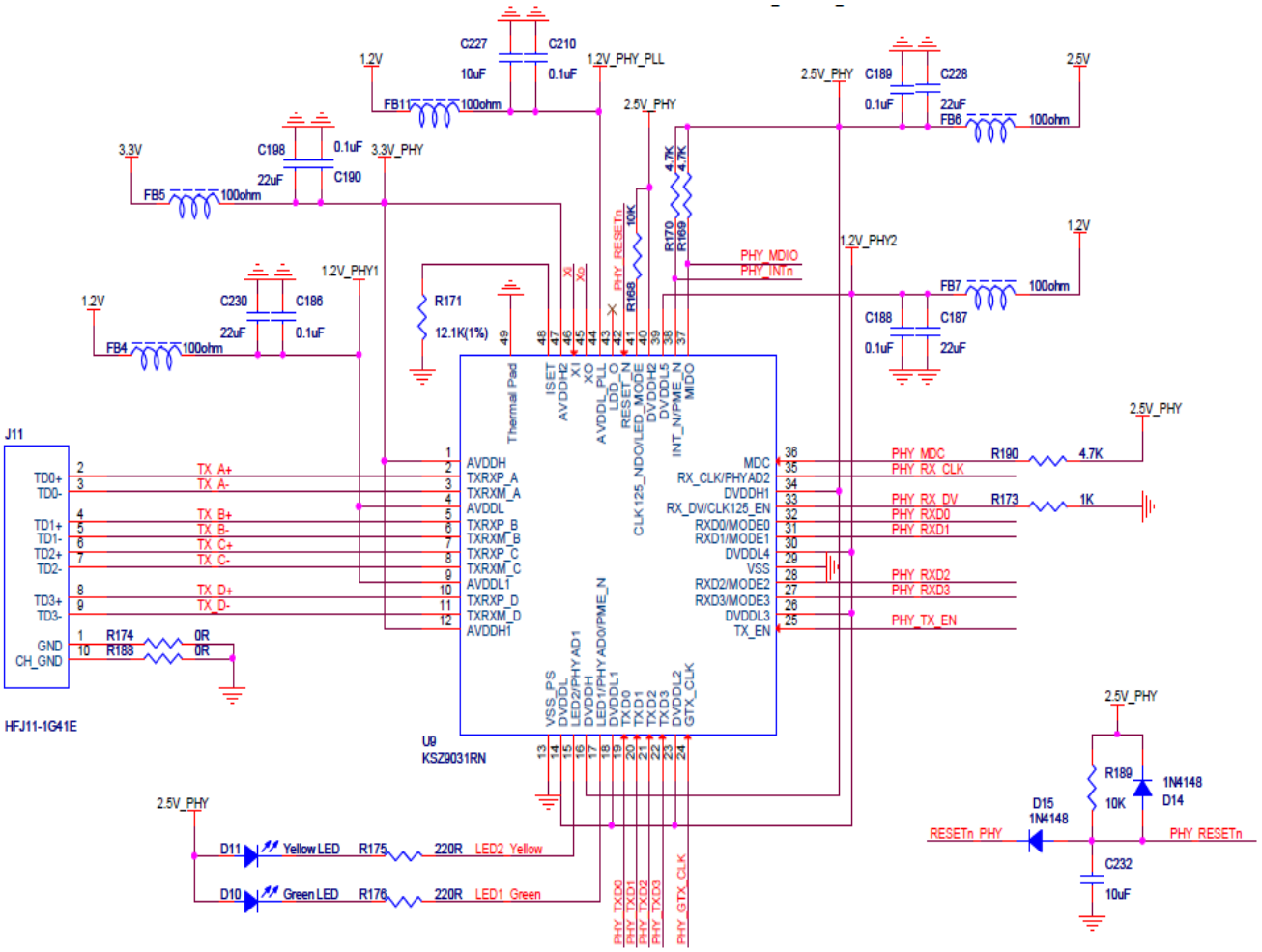


3.2.4.2 Ethernet interface

Ethernet connector is showed in the picture blew:

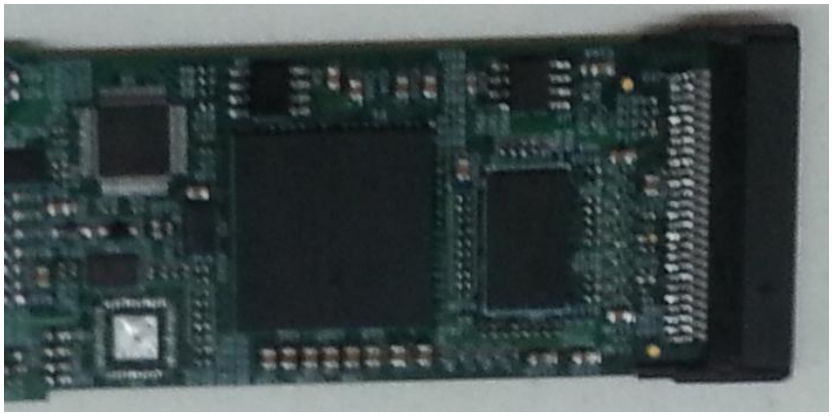


SCH of Ethernet interface:

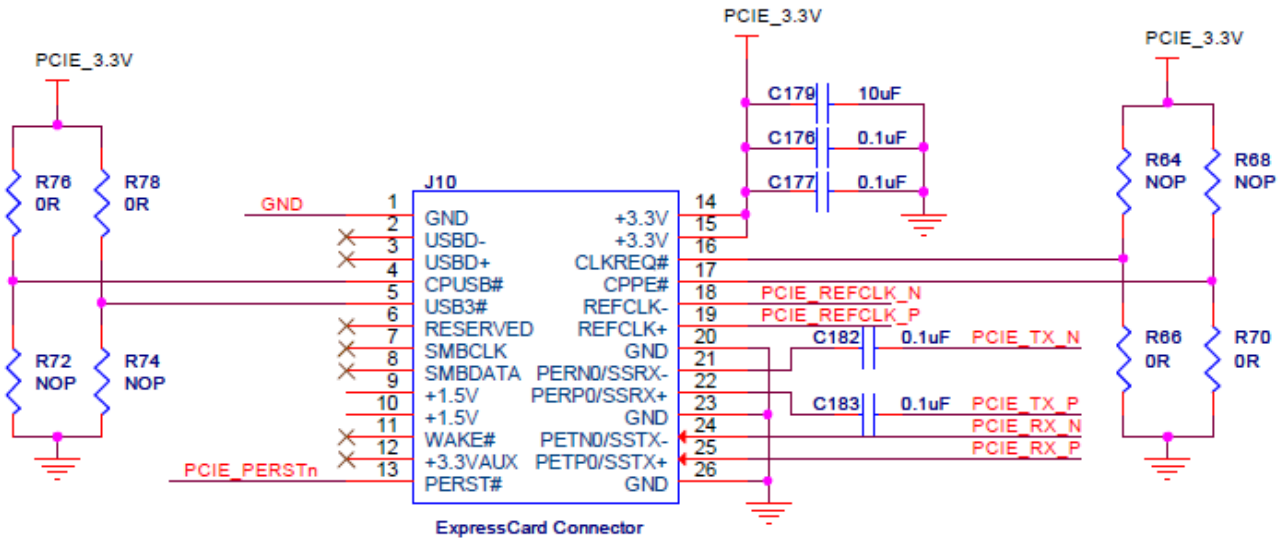


3.2.4.3 ExpressCard 34（PCIe）interface

ExpressCard 34（PCIe）connector is showed in the picture below:

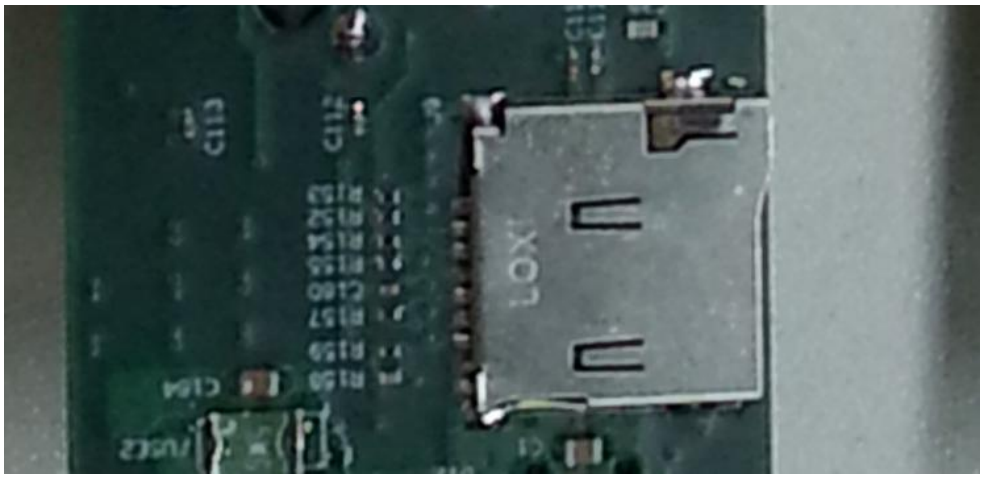


Schematic of ExpressCard 34（PCIe）connection:

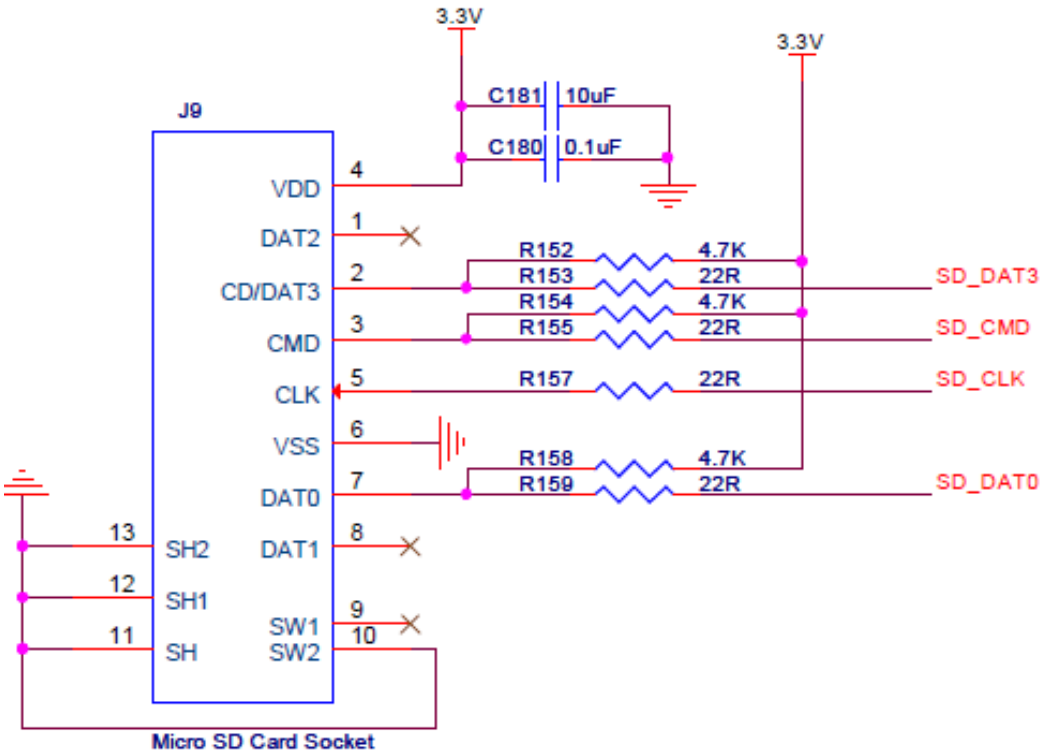


3.2.4.4 Micro-SD

Micro-SD connector is showed in the picture below:

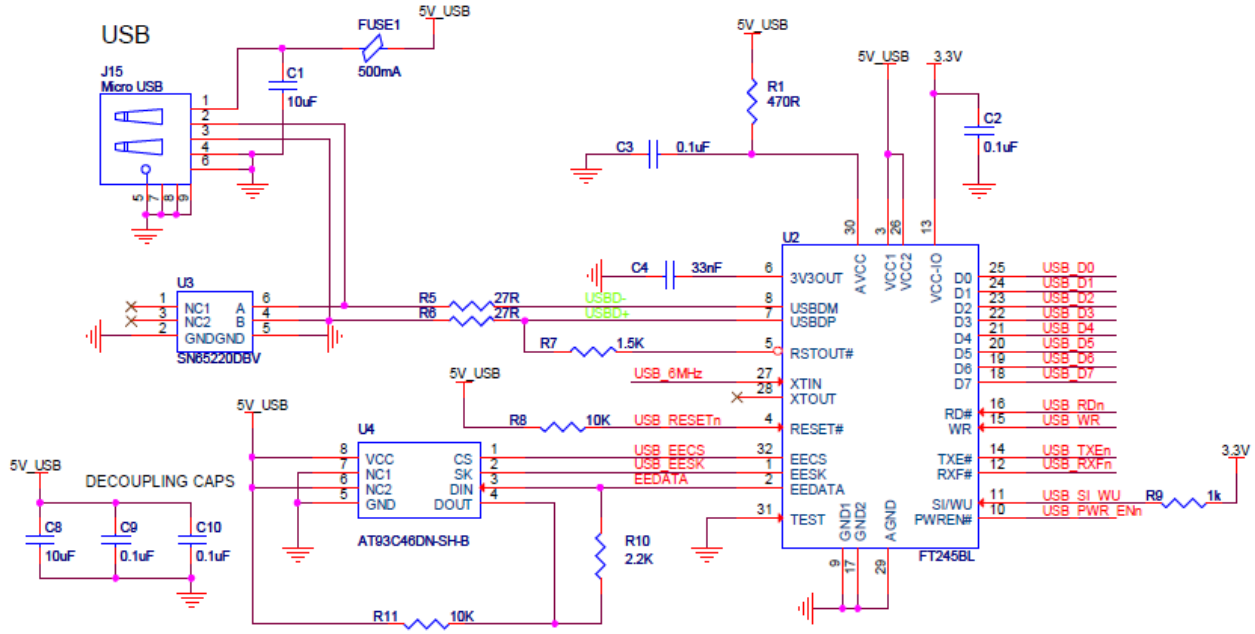


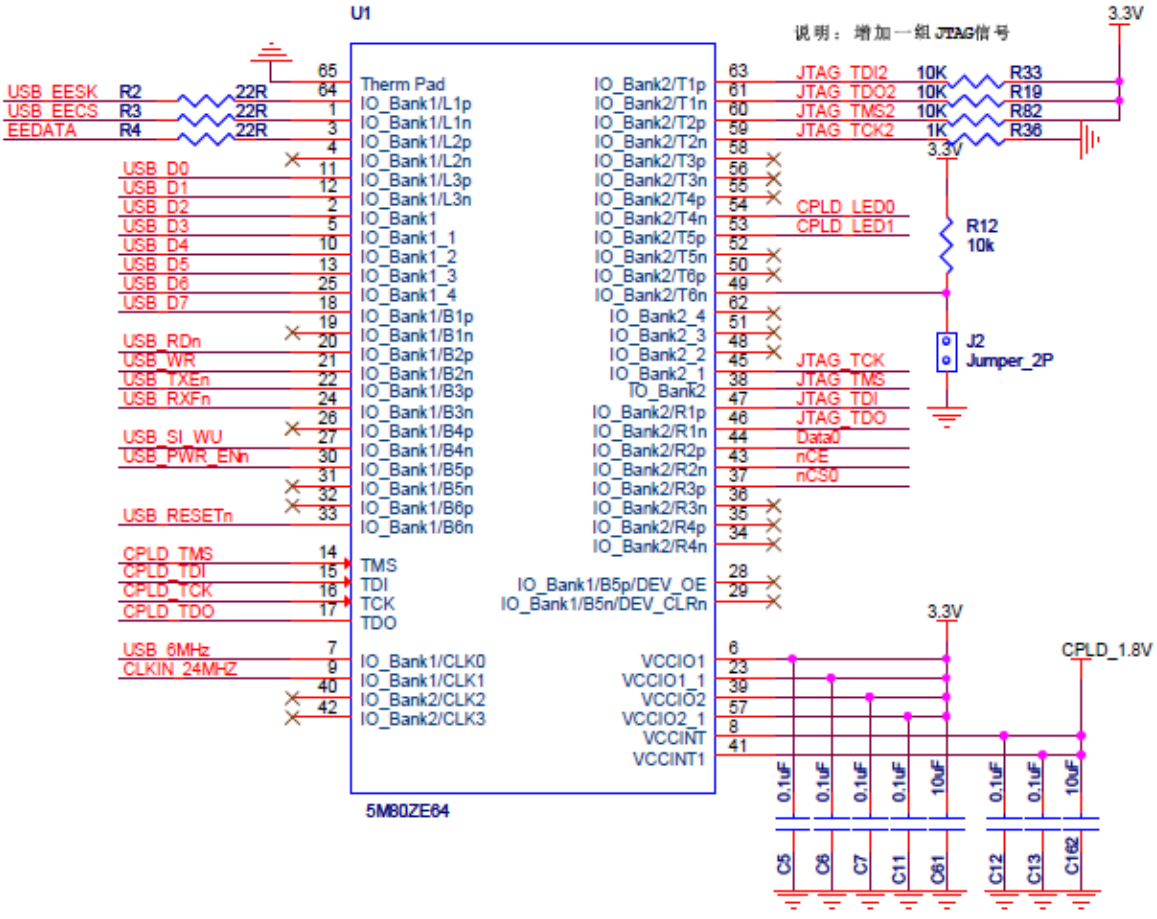
Schematic of Micro-SD:



3.2.4.5 Embedded USB Blaster Function

Schematic of Embedded USB Blaster:





Embedded USB Blaster jumper (J2) configuration:

J2	USB Blaster Mode	Comment
Shorted	Only for FPGA on board	
Opened	JTAG for FPGA/CPLD off board	Need to connect expansion board to J3

4 Lab Instructions

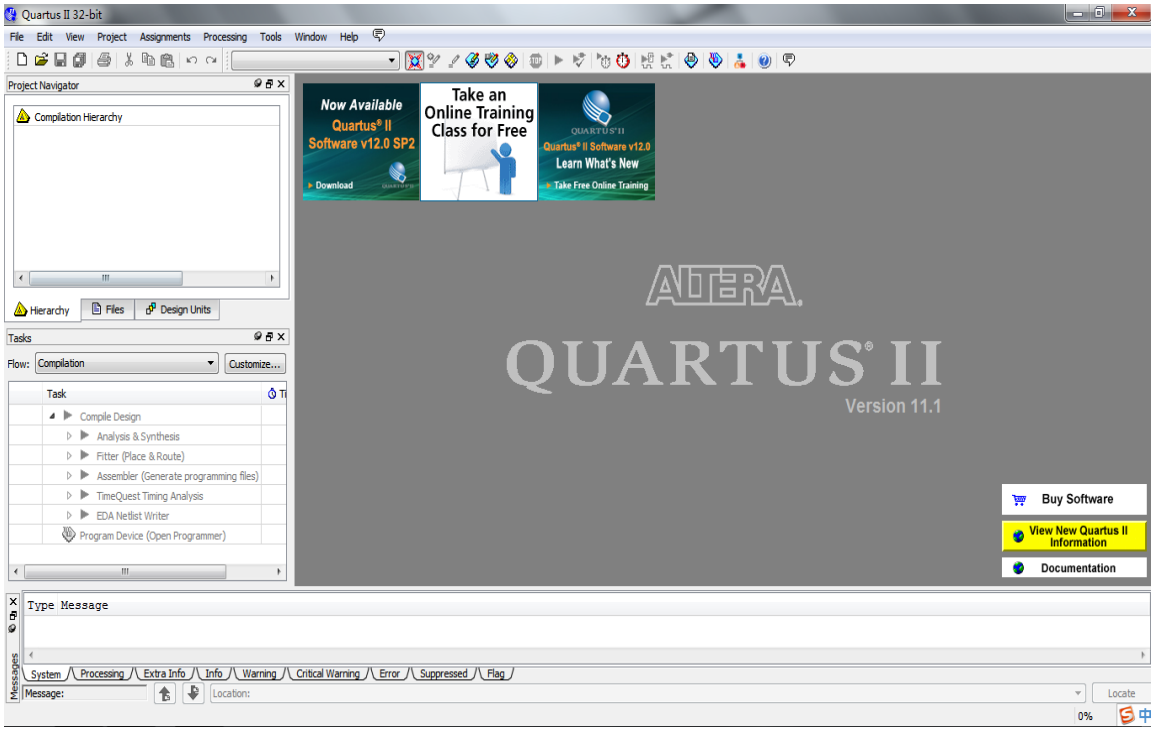
4.1 Lab 1

4.1.1 Objective

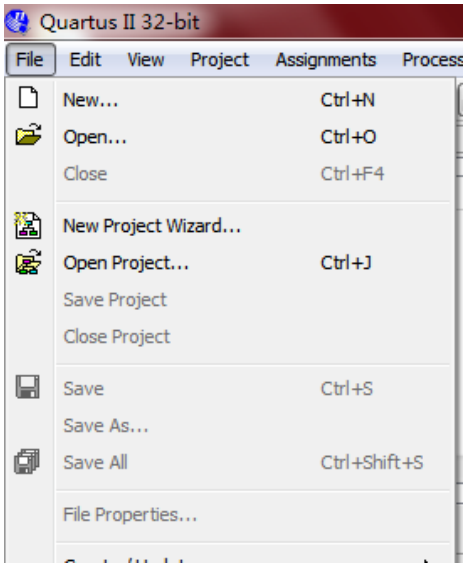
The following lab exercise is to demonstrate LED flashing after complete setup of EasyGX hardware and Quartus II software.

4.1.2 Step by step

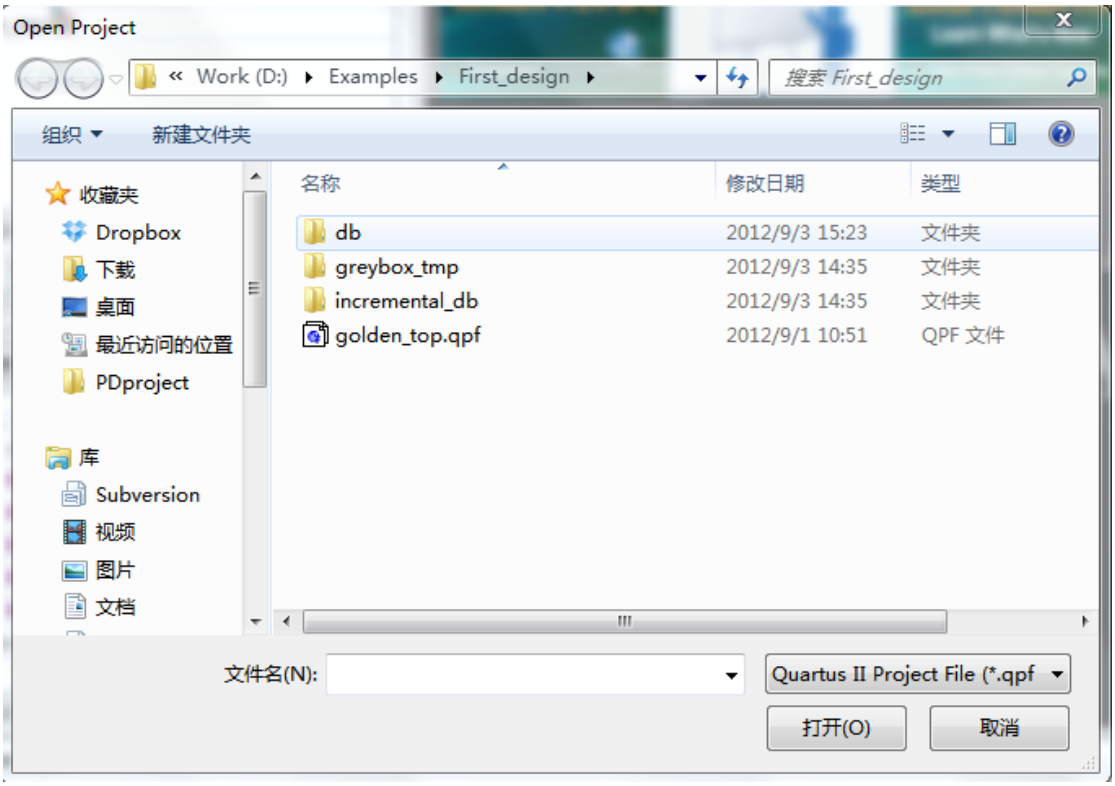
Launch Quartus II.



File -> Open Project.

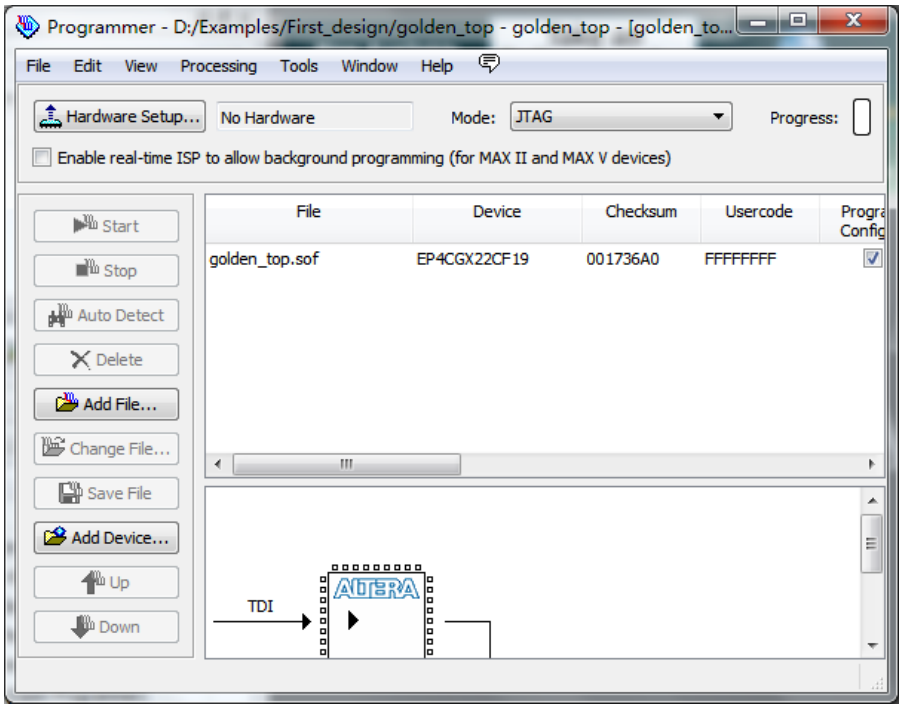


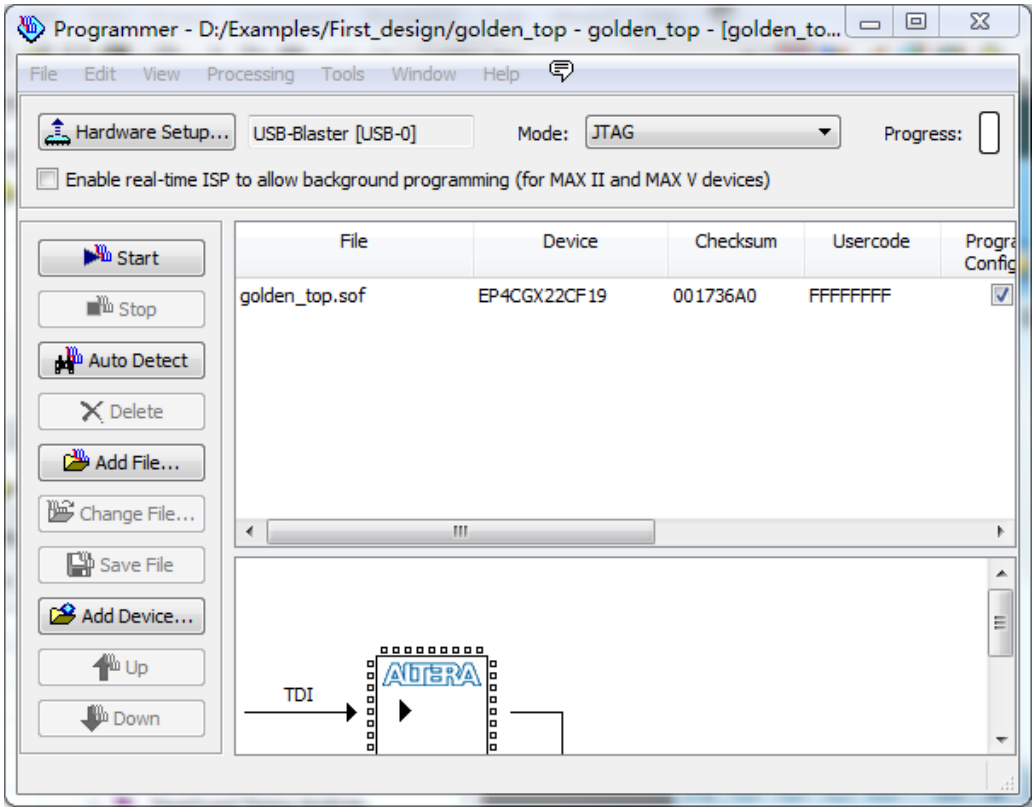
Find First_design directory，open .qpf file.



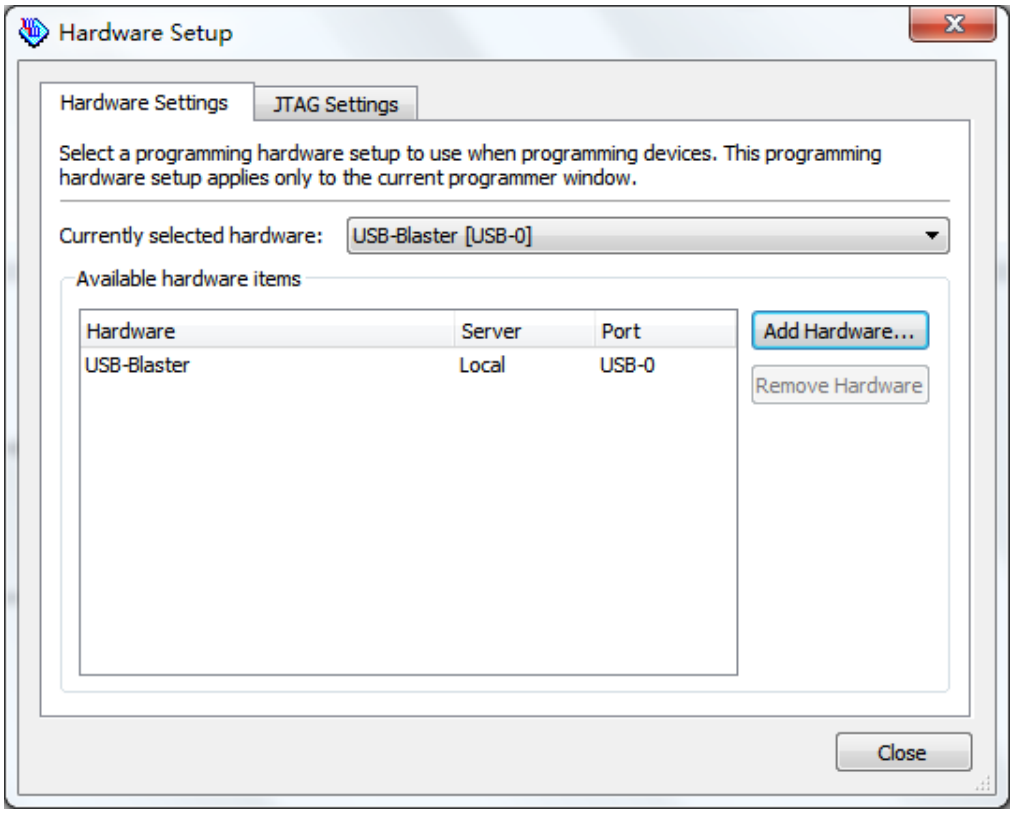
Click the “Programmer” icon in the toolbar or select Tools->Programmer.

If occur situation below, click “Hardware Setup” on the left-up corner.

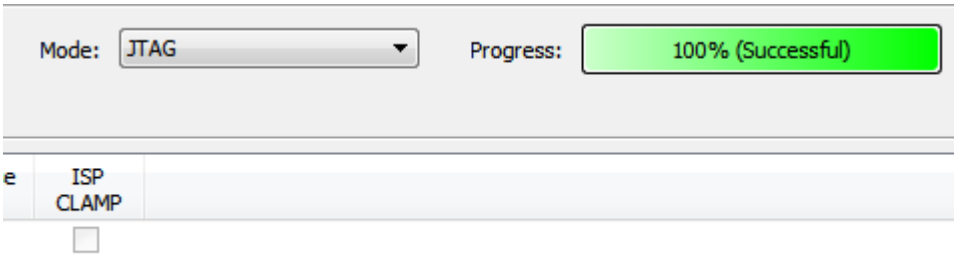




Select “USB_Blaster[USB-0]” in the drop-down box，then click “Close”.



Click “Start” in the left to start programming. You can see below if it is successful.



Once it is programmed successfully, you can see D6~D9 LED flashing in binary-sequential order.

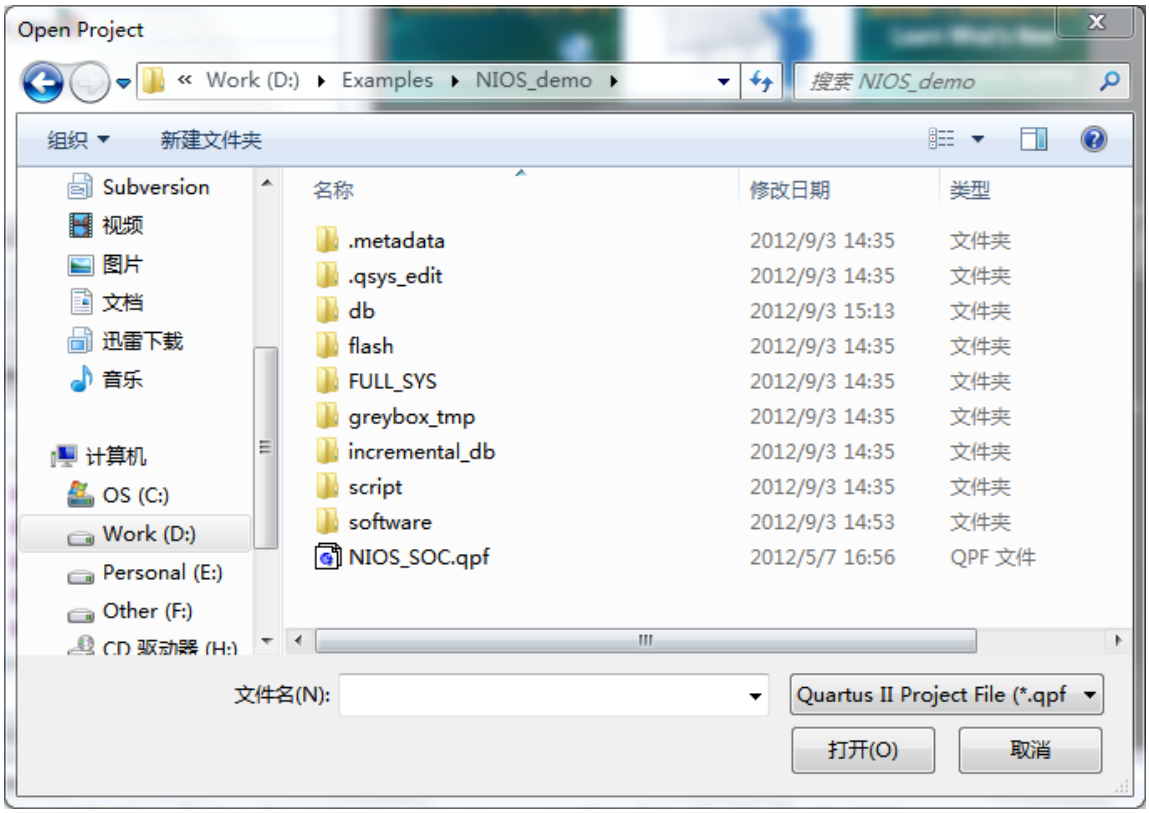
4.2 Lab 2

4.2.1 Objective

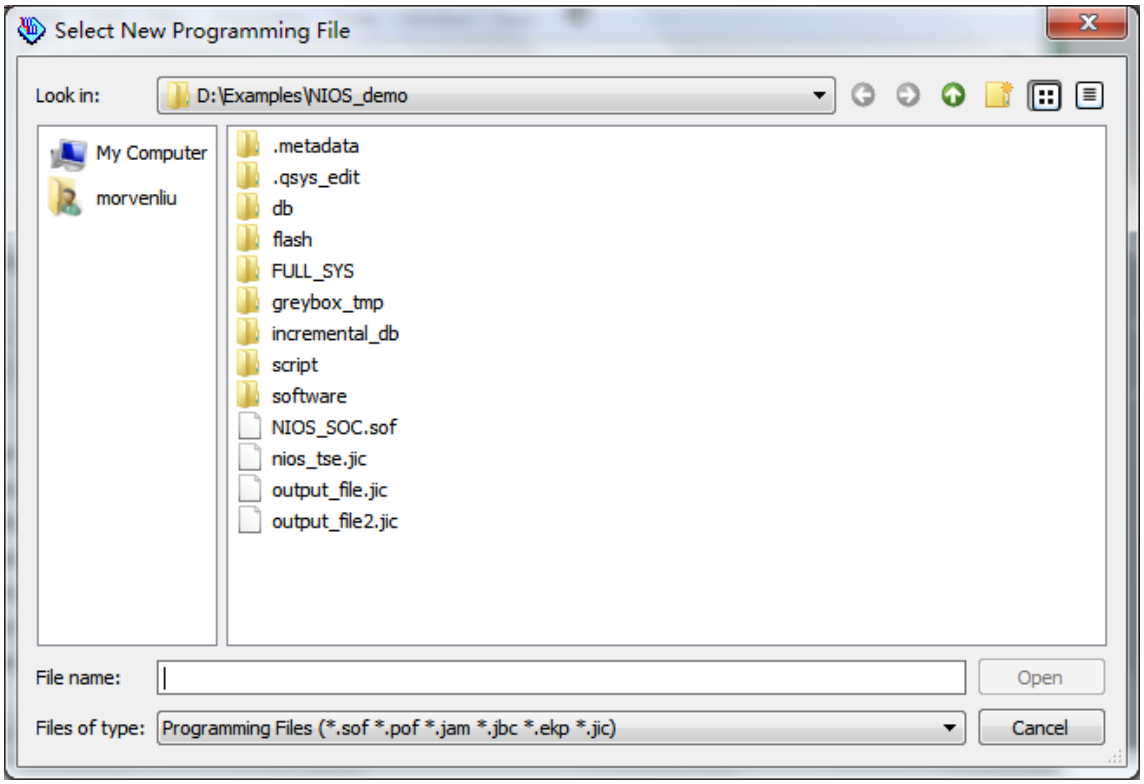
The following lab exercise allows you to use NIOS II simple socket server to toggle LED. It also utilized Gigabit Ethernet port as a server controller.

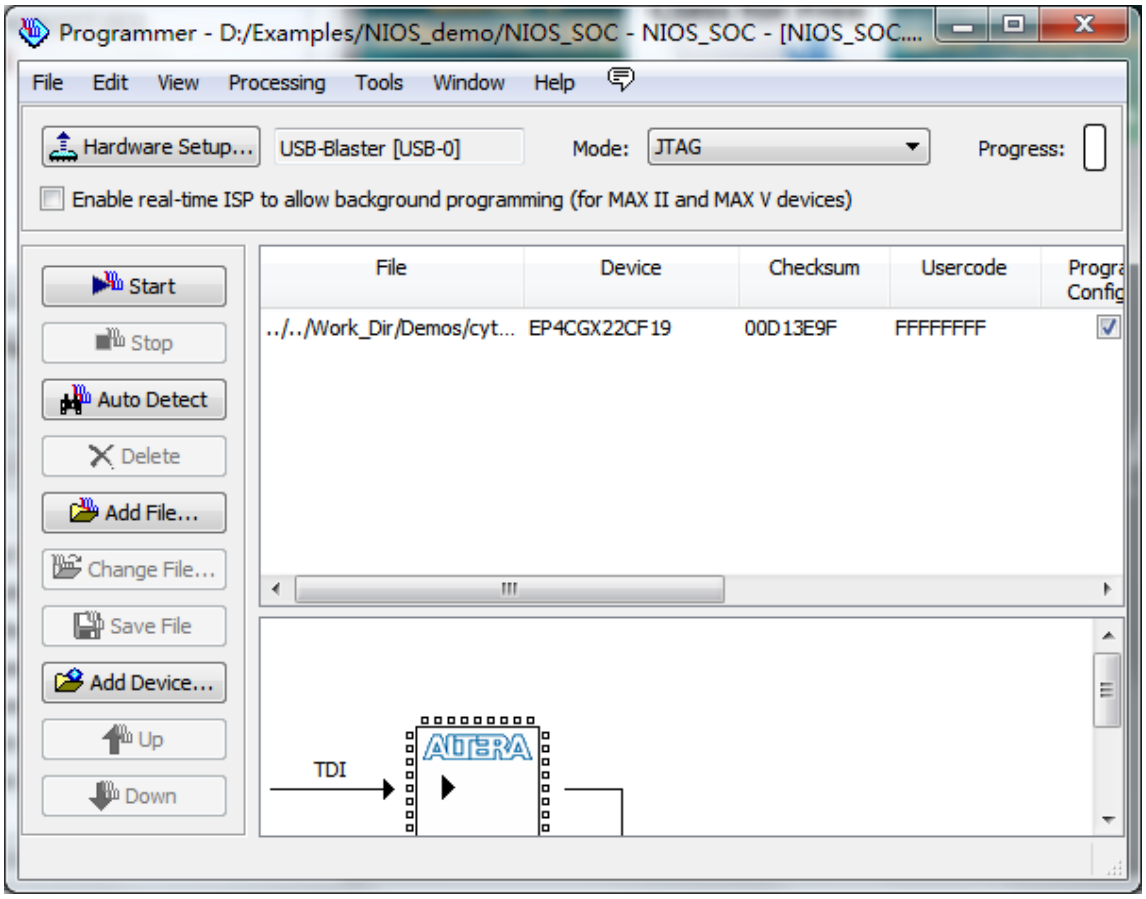
4.2.2 Step by step

Open Examples from “NIOS_demo” folder with project “NIOS_SOC.qpf” in Quartus II

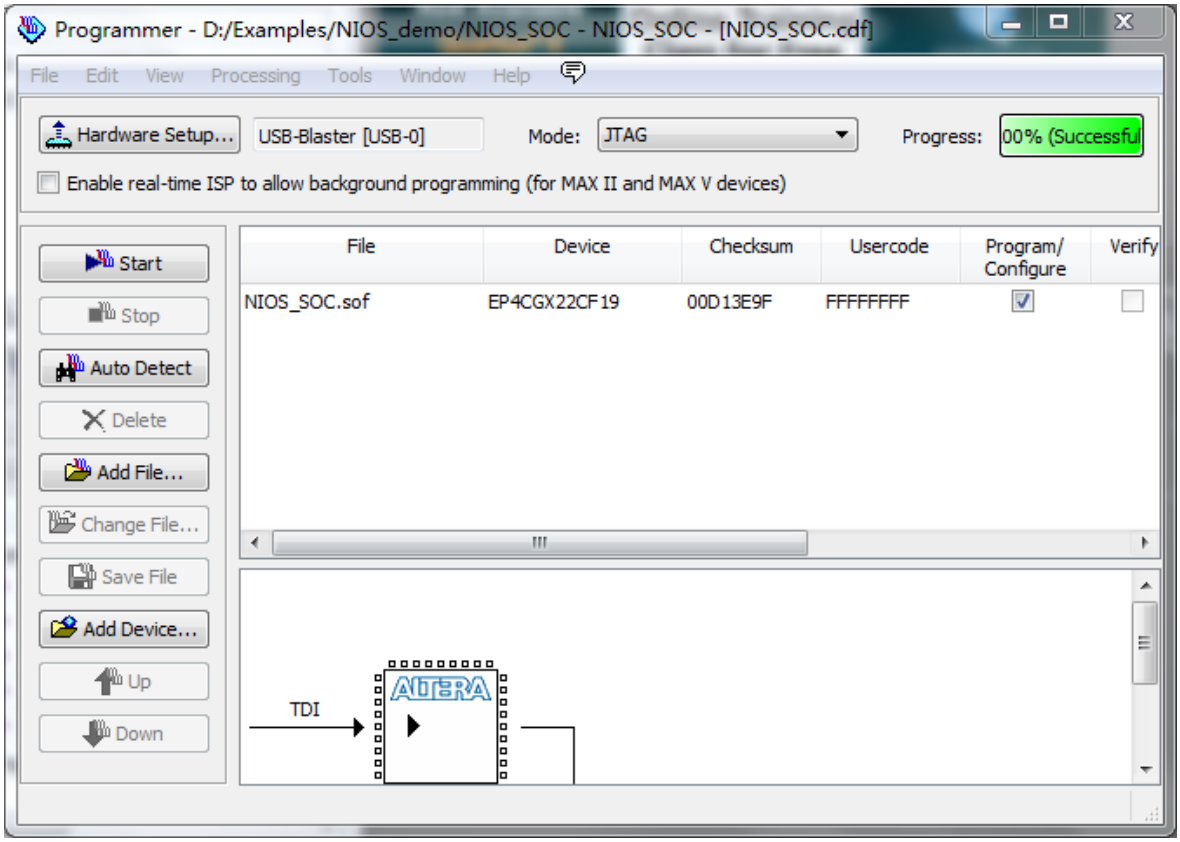


Then select programmer. Double click the file in the “File” item, choose the file “NIOS_SOC.sof” for programming.


Select New Programming File
Look in:
D:\Examples\NIOS_demo
My Computer
morvenliu
.metadata
.qsys_edit
db
flash
FULL_SYS
greybox_tmp
incremental_db
script
software
NIOS_SOC.sof
nios_tse.jic
output_file.jic
output_file2.jic
File name:
Open
Files of type:
Programming Files (*.sof *.pof *.jam *.jbc *.ekp *.jic)
Cancel

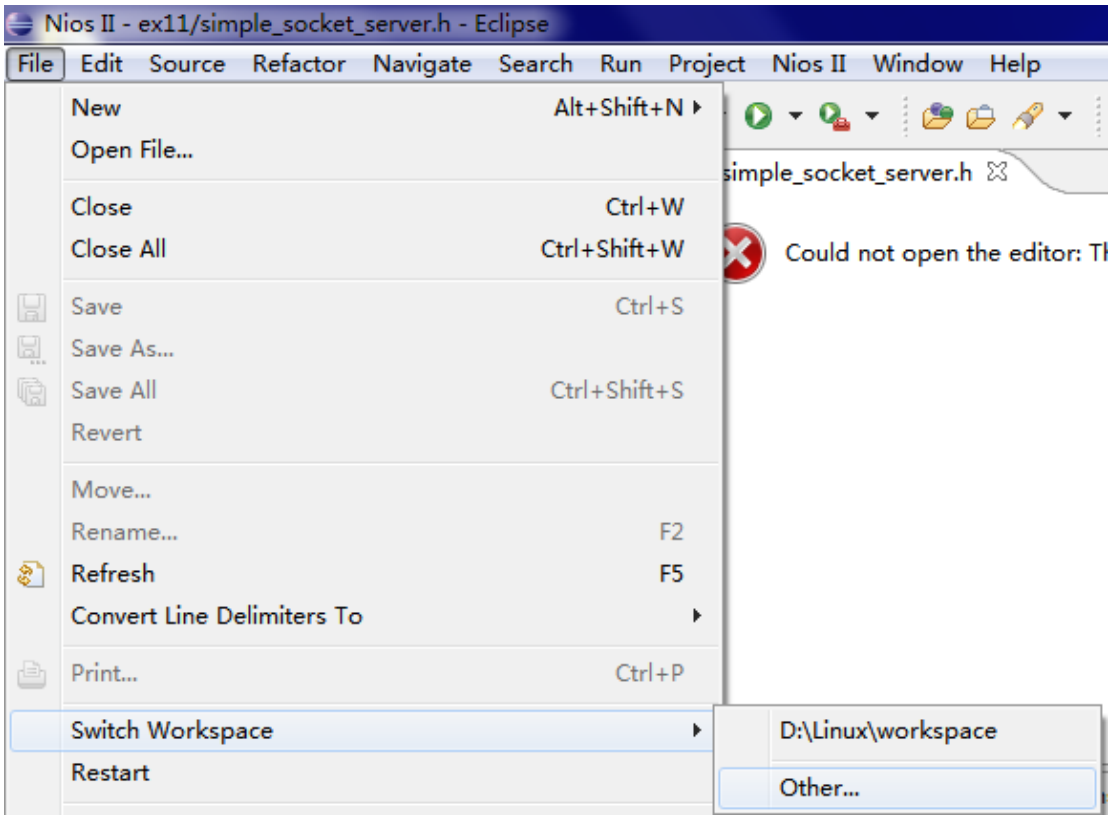

Programmer - D:/Examples/NIOS_demo/NIOS_SOC - NIOS_SOC - [NIOS_SOC....
File
Edit
View
Processing
Tools
Window
Help
Hardware Setup...
USB-Blaster [USB-0]
Mode:
JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Progra
Config
../../Work_Dir/Demos/cyt...
EP4CGX22CF19
00D13E9F
FFFFFFFF
TDI

Then, click “Start” to program. Showed as below when it is completed.

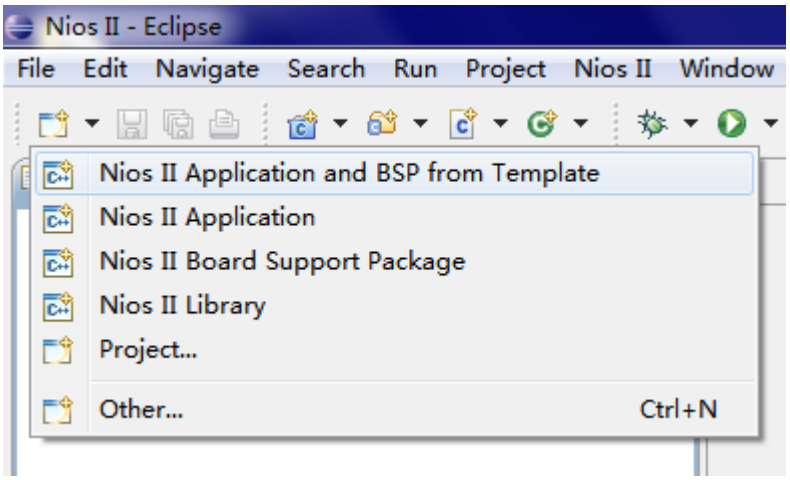


Launch Nios II in the program list, suggest to run it under PC-administrator privilege.

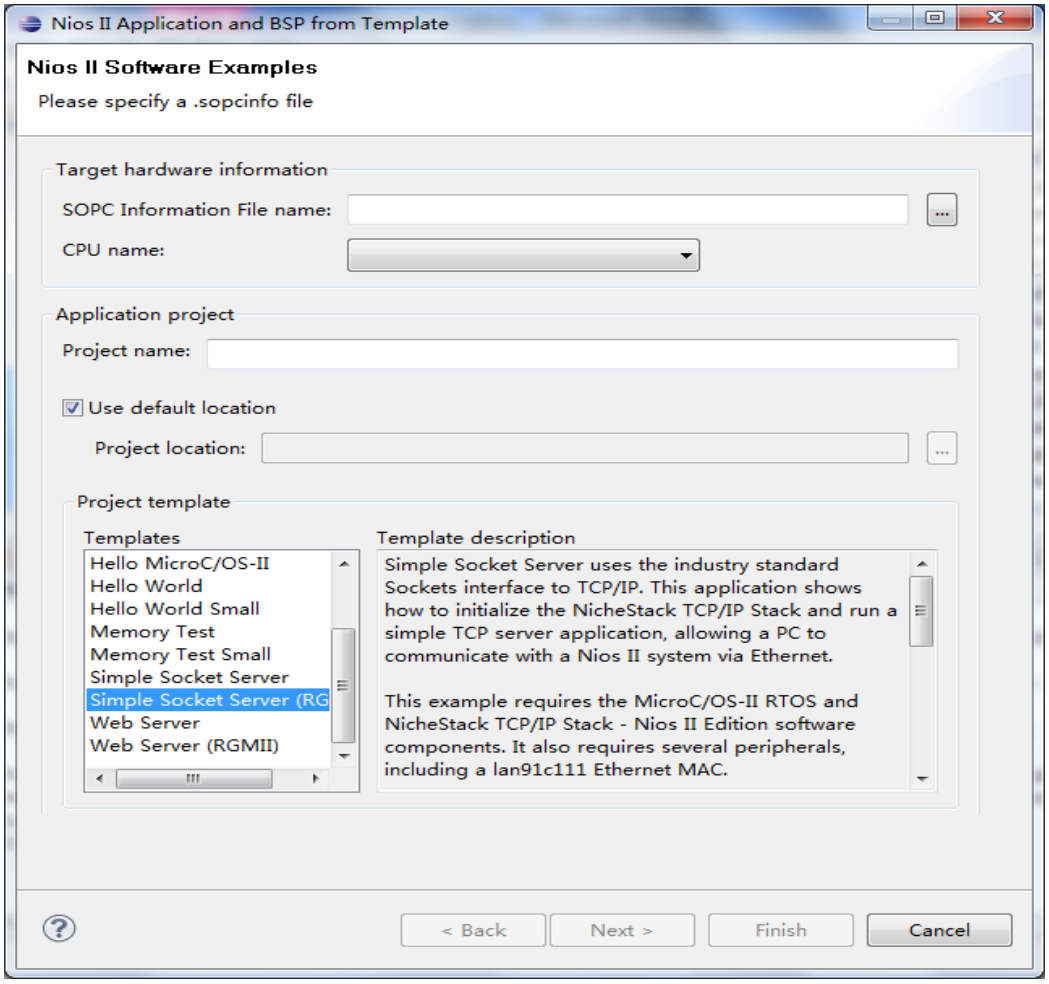
File->Switch Workspace->Other，select directory of the Lab example project.

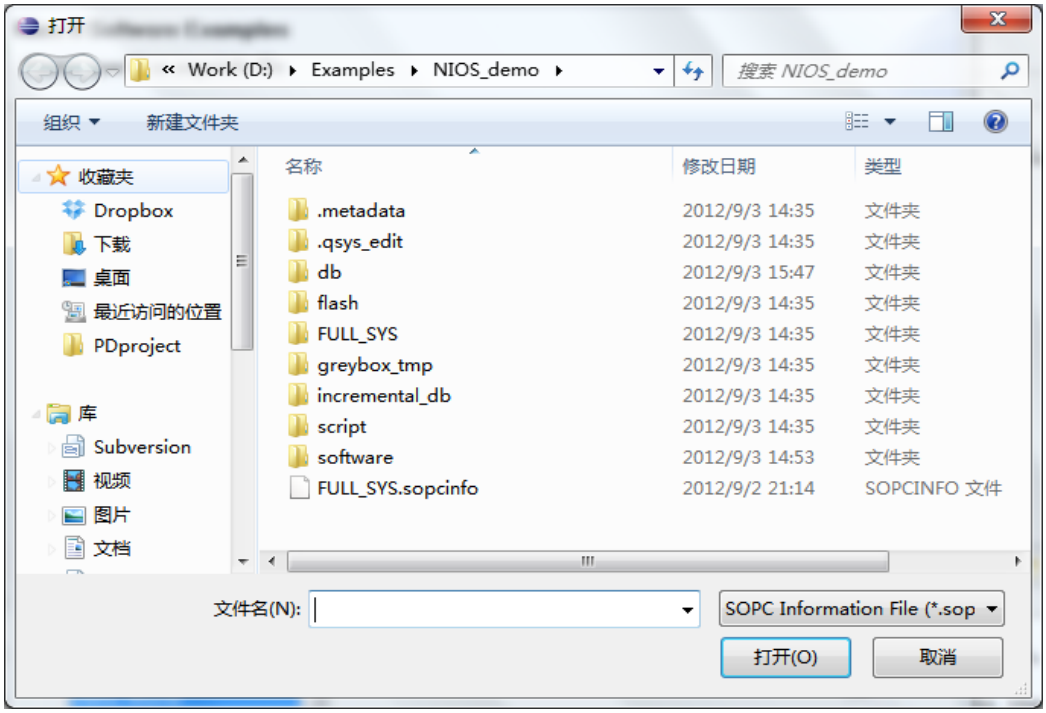


New create one project by click “NiosII Application and BSP from Template”.



Select “SOPC”, fill the “Project Name”, and choose “Template” as “Simple Socket Server (RG…”.





Modify file “simple_socket_server.h” as below.

simple_socket_server.h

```
 * these values are only a valid default on networks with DHCP s
 *
 * If DHCP will not be used, select valid static IP addresses he
 *           IP: 192.168.1.234
 *      Gateway: 192.168.1.1
 *  Subnet Mask: 255.255.255.0
 */
#define IPADDR0   0
#define IPADDR1   0
#define IPADDR2   0
#define IPADDR3   0

#define GWADDR0   0
#define GWADDR1   0
#define GWADDR2   0
#define GWADDR3   0
```

simple_socket_server.h

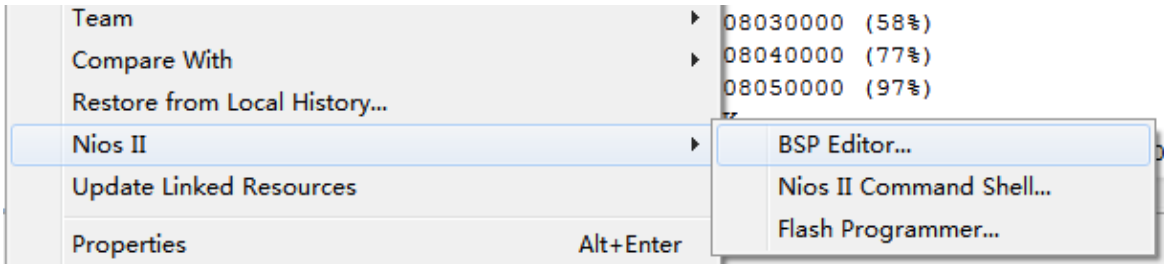
```
 * these values are only a valid default on networks with DHCP s
 *
 * If DHCP will not be used, select valid static IP addresses he
 *           IP: 192.168.1.234
 *      Gateway: 192.168.1.1
 *  Subnet Mask: 255.255.255.0
 */
#define IPADDR0   192
#define IPADDR1   168
#define IPADDR2   1
#define IPADDR3   234

#define GWADDR0   192
#define GWADDR1   168
#define GWADDR2   1
#define GWADDR3   1
```

Open network_utilities.c, search “ser_num = get_serial_number()” and replace it using “ ser_num = 123456789” as below.

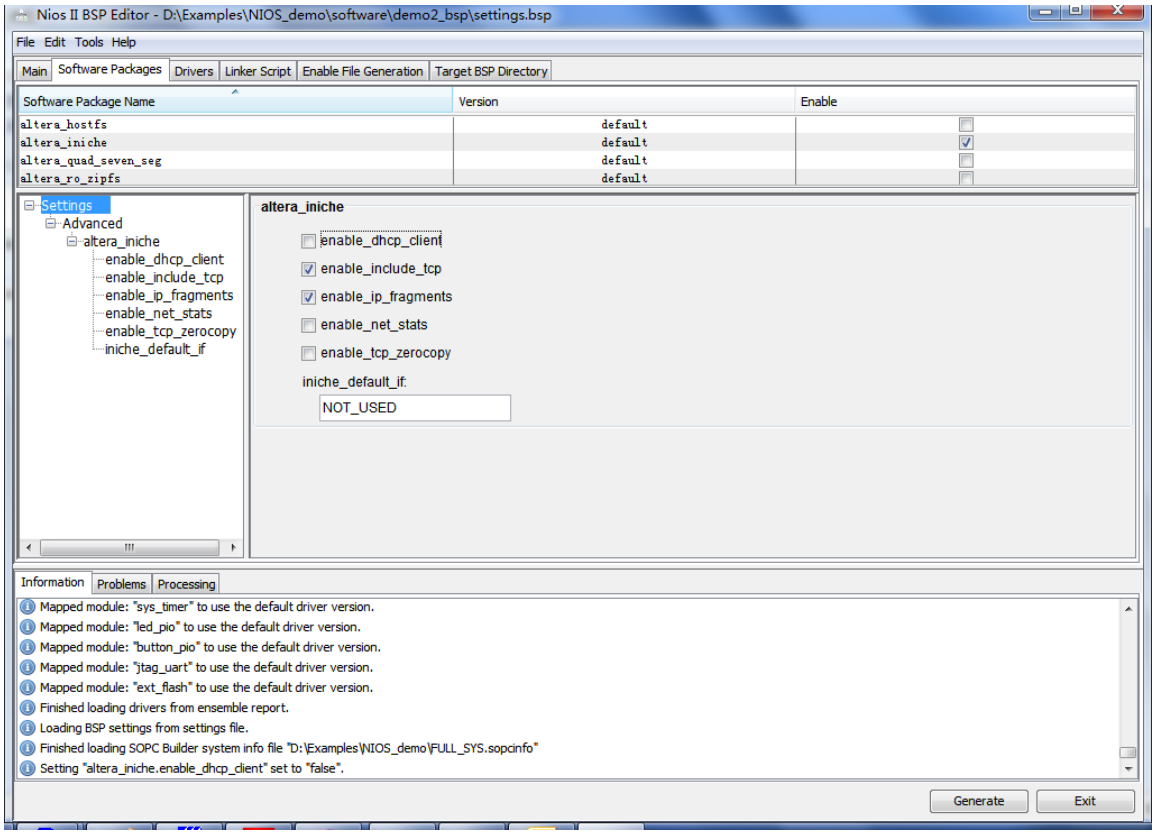
simple_socket_server.h | network_utilities.c

```
    printf("Can't read the MAC address from your board (this prc
    printf("that your flash was erased). We will assign you a MA
    printf("static network settings\n\n");

    //ser_num = get_serial_number();
    ser_num = 123456789;

    if (ser_num)
    {
        /* This says the image is safe */
        flash_content[0] = 0xfe;
        flash_content[1] = 0x5a;
        flash_content[2] = 0x0;
        flash_content[3] = 0x0;
```

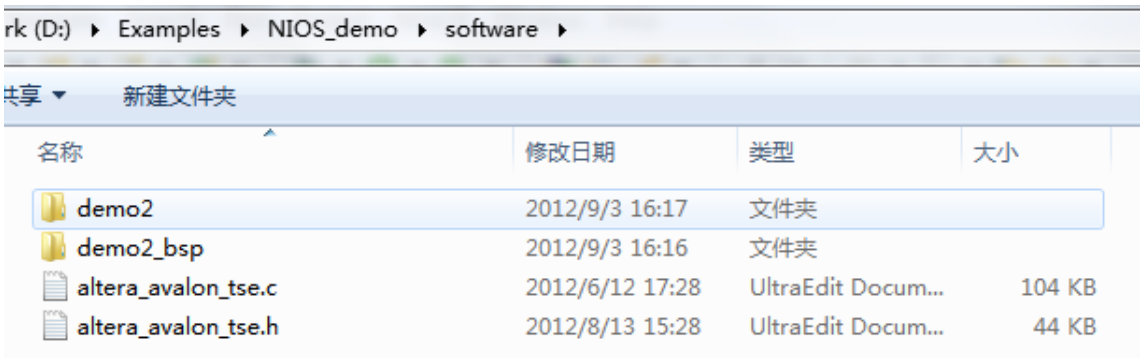
Right click on the project, and select NiosII->BSP Editor.

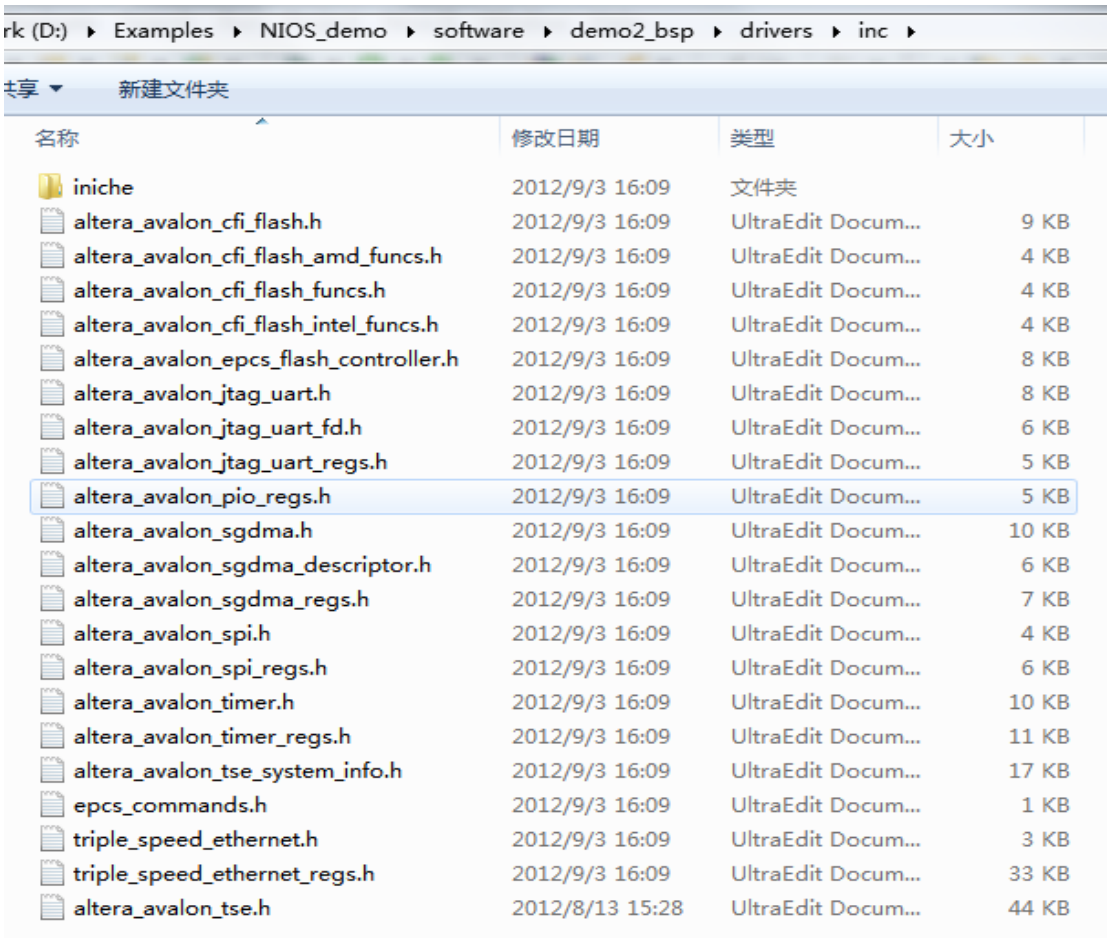


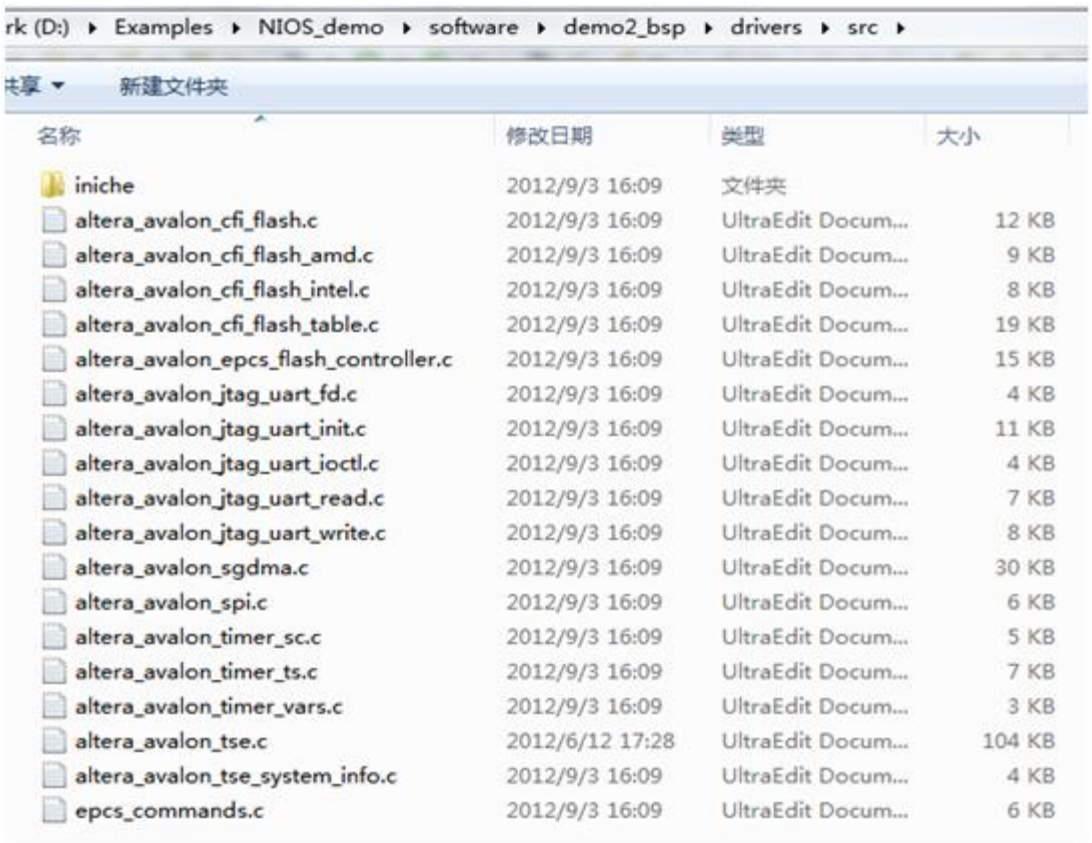
Click “Software Packages” label, remove “enable_dhcp_client” option. Then click “Generate”.



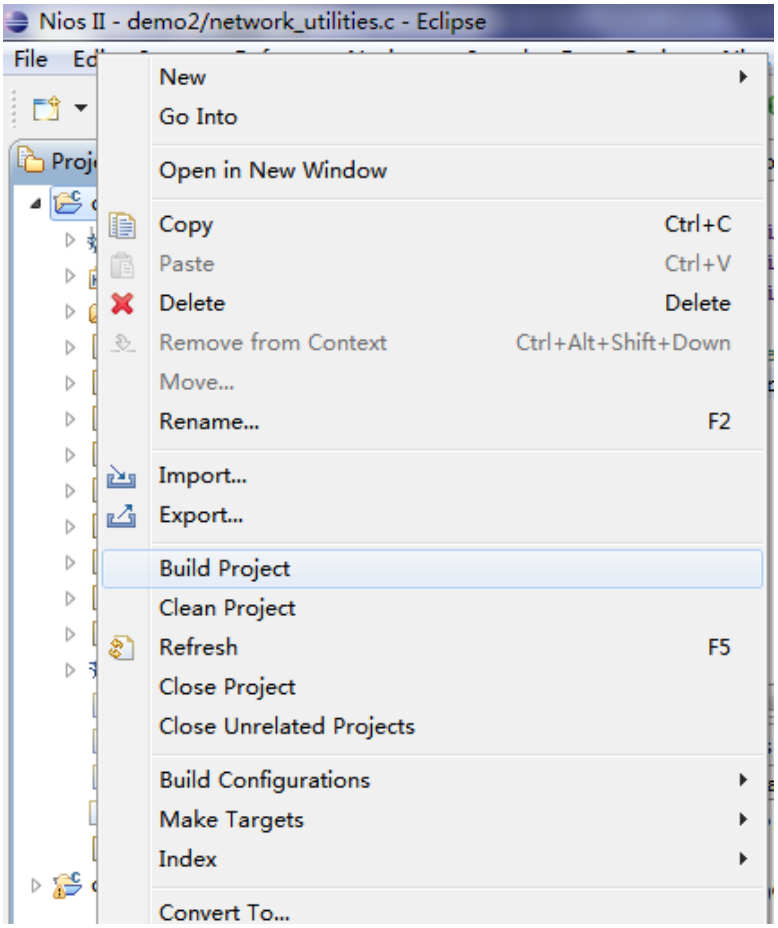
There’re 2 files under this directory, copy .h file to “demo2_bsp –>drivers->inc”, and copy .c file to “demo2_bsp –>drivers->src”, replace the original files.



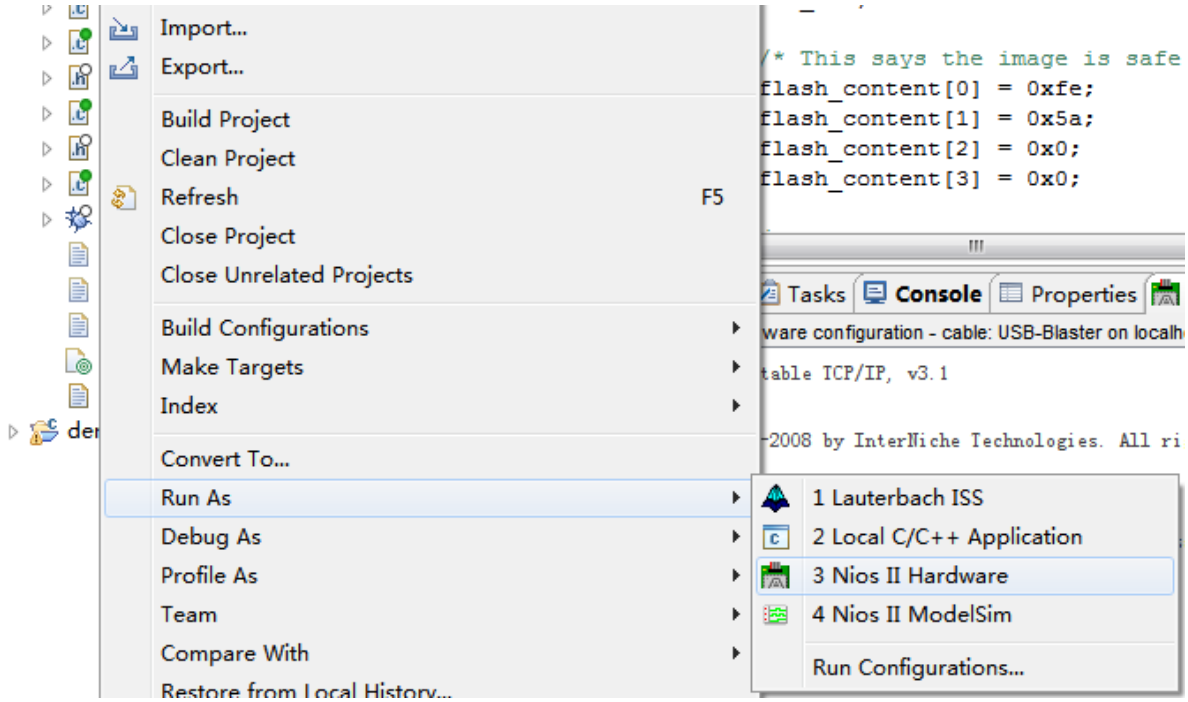

rk (D:) ▸ Examples ▸ NIOS_demo ▸ software ▸ demo2_bsp ▸ drivers ▸ inc ▸
共享 ▾ 新建文件夹
名称 修改日期 类型 大小
iniche 2012/9/3 16:09 文件夹
altera_avalon_cfi_flash.h 2012/9/3 16:09 UltraEdit Docum... 9 KB
altera_avalon_cfi_flash_amd_funcs.h 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_cfi_flash_funcs.h 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_cfi_flash_intel_funcs.h 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_epcs_flash_controller.h 2012/9/3 16:09 UltraEdit Docum... 8 KB
altera_avalon_jtag_uart.h 2012/9/3 16:09 UltraEdit Docum... 8 KB
altera_avalon_jtag_uart_fd.h 2012/9/3 16:09 UltraEdit Docum... 6 KB
altera_avalon_jtag_uart_regs.h 2012/9/3 16:09 UltraEdit Docum... 5 KB
altera_avalon_pio_regs.h 2012/9/3 16:09 UltraEdit Docum... 5 KB
altera_avalon_sgdma.h 2012/9/3 16:09 UltraEdit Docum... 10 KB
altera_avalon_sgdma_descriptor.h 2012/9/3 16:09 UltraEdit Docum... 6 KB
altera_avalon_sgdma_regs.h 2012/9/3 16:09 UltraEdit Docum... 7 KB
altera_avalon_spi.h 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_spi_regs.h 2012/9/3 16:09 UltraEdit Docum... 6 KB
altera_avalon_timer.h 2012/9/3 16:09 UltraEdit Docum... 10 KB
altera_avalon_timer_regs.h 2012/9/3 16:09 UltraEdit Docum... 11 KB
altera_avalon_tse_system_info.h 2012/9/3 16:09 UltraEdit Docum... 17 KB
epcs_commands.h 2012/9/3 16:09 UltraEdit Docum... 1 KB
triple_speed_ethernet.h 2012/9/3 16:09 UltraEdit Docum... 3 KB
triple_speed_ethernet_regs.h 2012/9/3 16:09 UltraEdit Docum... 33 KB
altera_avalon_tse.h 2012/8/13 15:28 UltraEdit Docum... 44 KB


rk (D:) ▸ Examples ▸ NIOS_demo ▸ software ▸ demo2_bsp ▸ drivers ▸ src ▸
共享 ▾ 新建文件夹
名称 修改日期 类型 大小
iniche 2012/9/3 16:09 文件夹
altera_avalon_cfi_flash.c 2012/9/3 16:09 UltraEdit Docum... 12 KB
altera_avalon_cfi_flash_amd.c 2012/9/3 16:09 UltraEdit Docum... 9 KB
altera_avalon_cfi_flash_intel.c 2012/9/3 16:09 UltraEdit Docum... 8 KB
altera_avalon_cfi_flash_table.c 2012/9/3 16:09 UltraEdit Docum... 19 KB
altera_avalon_epcs_flash_controller.c 2012/9/3 16:09 UltraEdit Docum... 15 KB
altera_avalon_jtag_uart_fd.c 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_jtag_uart_init.c 2012/9/3 16:09 UltraEdit Docum... 11 KB
altera_avalon_jtag_uart_ioctl.c 2012/9/3 16:09 UltraEdit Docum... 4 KB
altera_avalon_jtag_uart_read.c 2012/9/3 16:09 UltraEdit Docum... 7 KB
altera_avalon_jtag_uart_write.c 2012/9/3 16:09 UltraEdit Docum... 8 KB
altera_avalon_sgdma.c 2012/9/3 16:09 UltraEdit Docum... 30 KB
altera_avalon_spi.c 2012/9/3 16:09 UltraEdit Docum... 6 KB
altera_avalon_timer_sc.c 2012/9/3 16:09 UltraEdit Docum... 5 KB
altera_avalon_timer_ts.c 2012/9/3 16:09 UltraEdit Docum... 7 KB
altera_avalon_timer_vars.c 2012/9/3 16:09 UltraEdit Docum... 3 KB
altera_avalon_tse.c 2012/6/12 17:28 UltraEdit Docum... 104 KB
altera_avalon_tse_system_info.c 2012/9/3 16:09 UltraEdit Docum... 4 KB
epcs_commands.c 2012/9/3 16:09 UltraEdit Docum... 6 KB

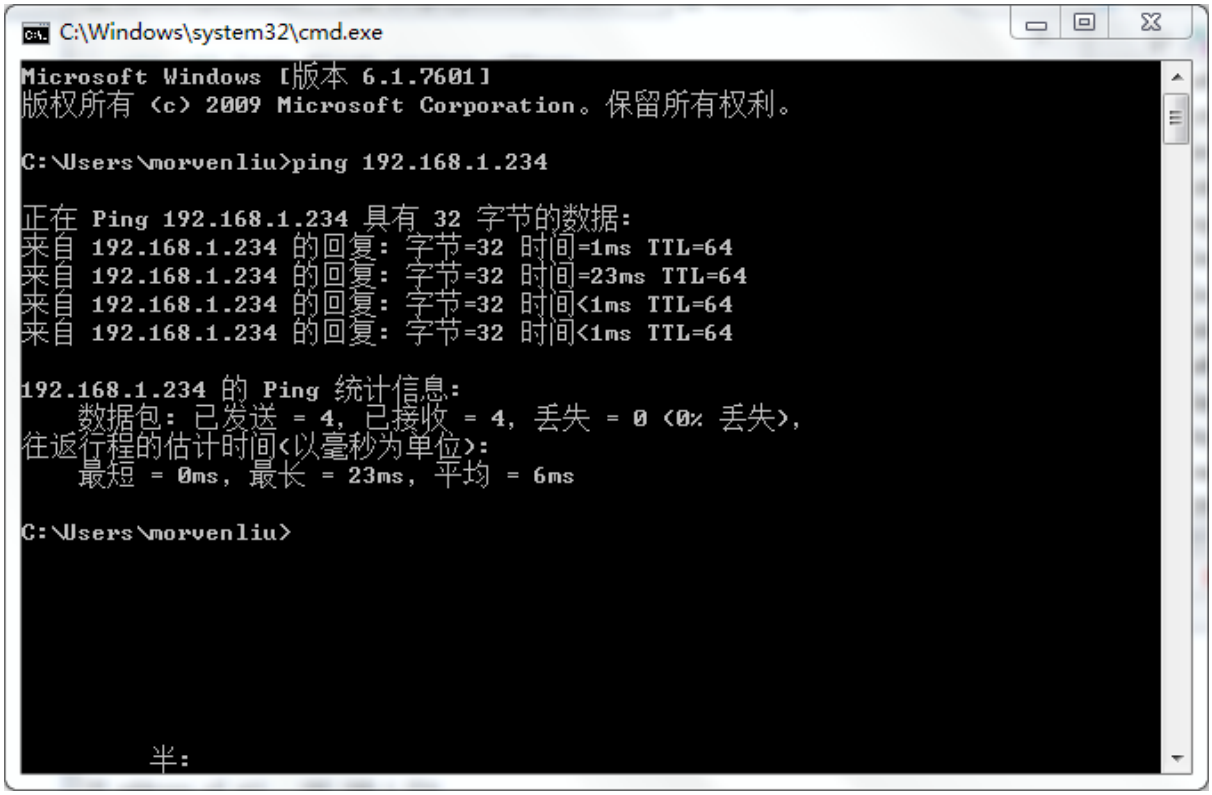
Build the project



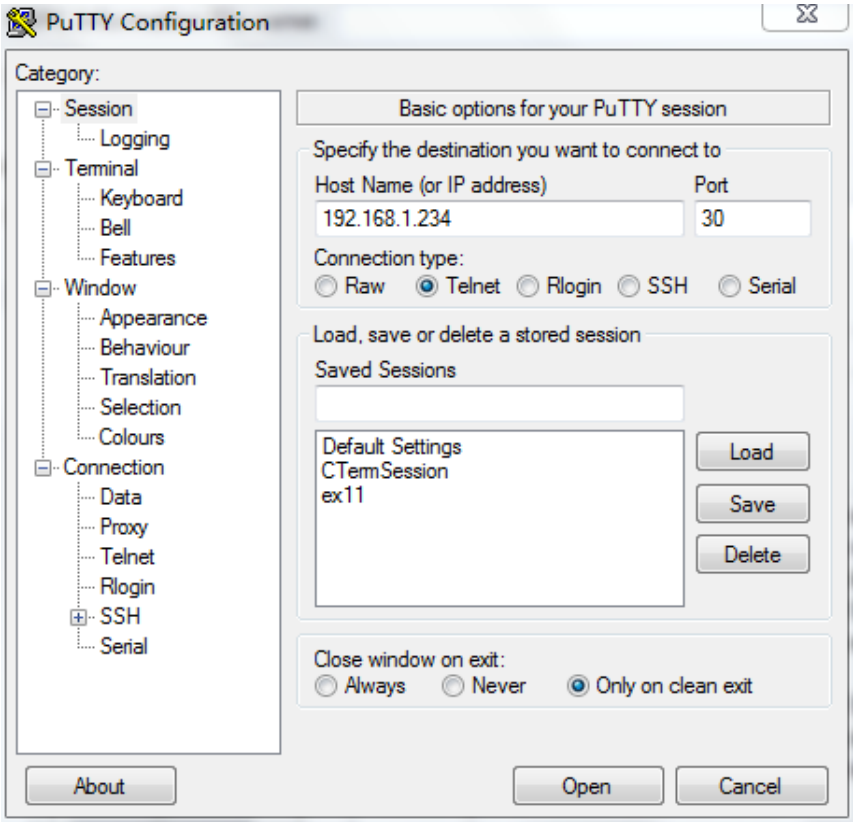
Right click and select “Run As->NiosII Hardware”



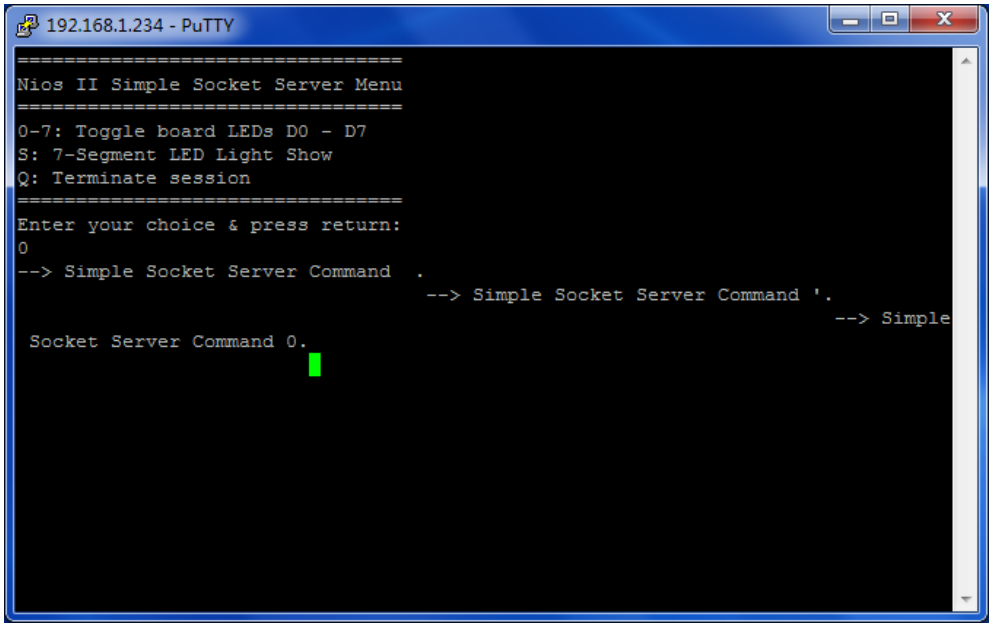
Run “cmd” , ping 192.168.1.234. Check if it can pass.



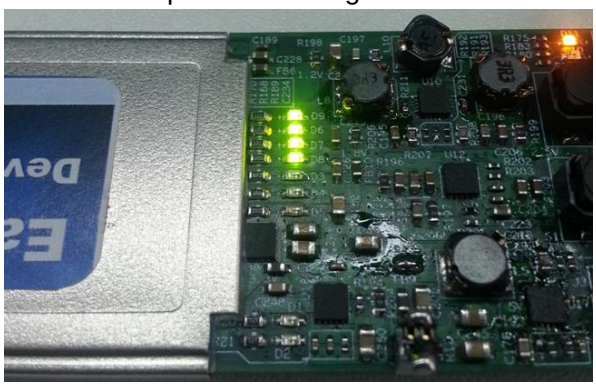
You can also use PuTTY to switch on/off LEDs on board. Launch PuTTY application, then configure it as below:



Click “Open”, then input a number range (0~3) to control D8，D7，D6，D9.



Reference capture of LED lights:



4.3 Lab 3

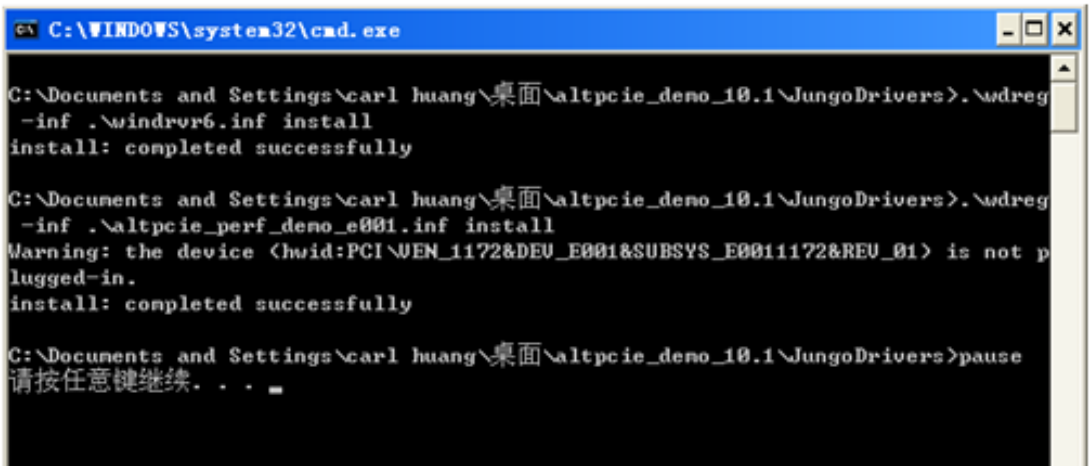
4.3.1 Objective

The following lab exercise is to demonstrate Cyclone IV GX PCIe hard IP and device data throughput performance. This design is based on Altera PCIe High Performance Reference Design (AN456)

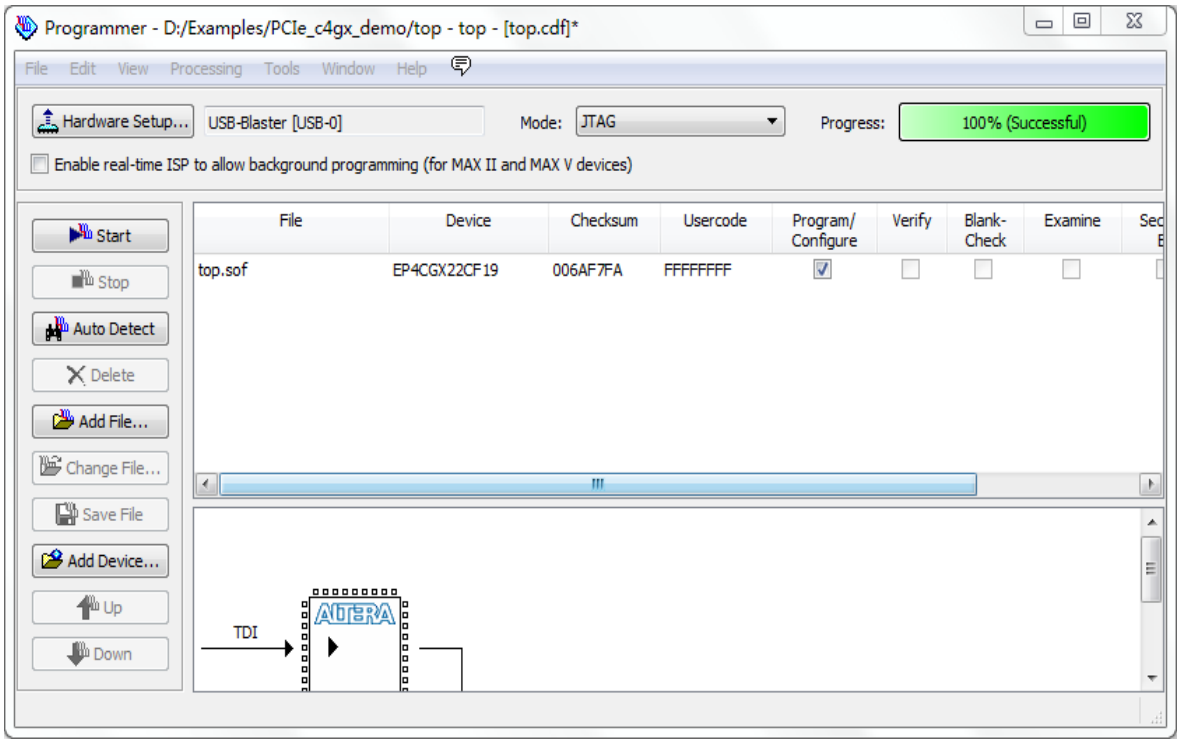
4.3.2 Step by step

Install driver. Run install.bat。

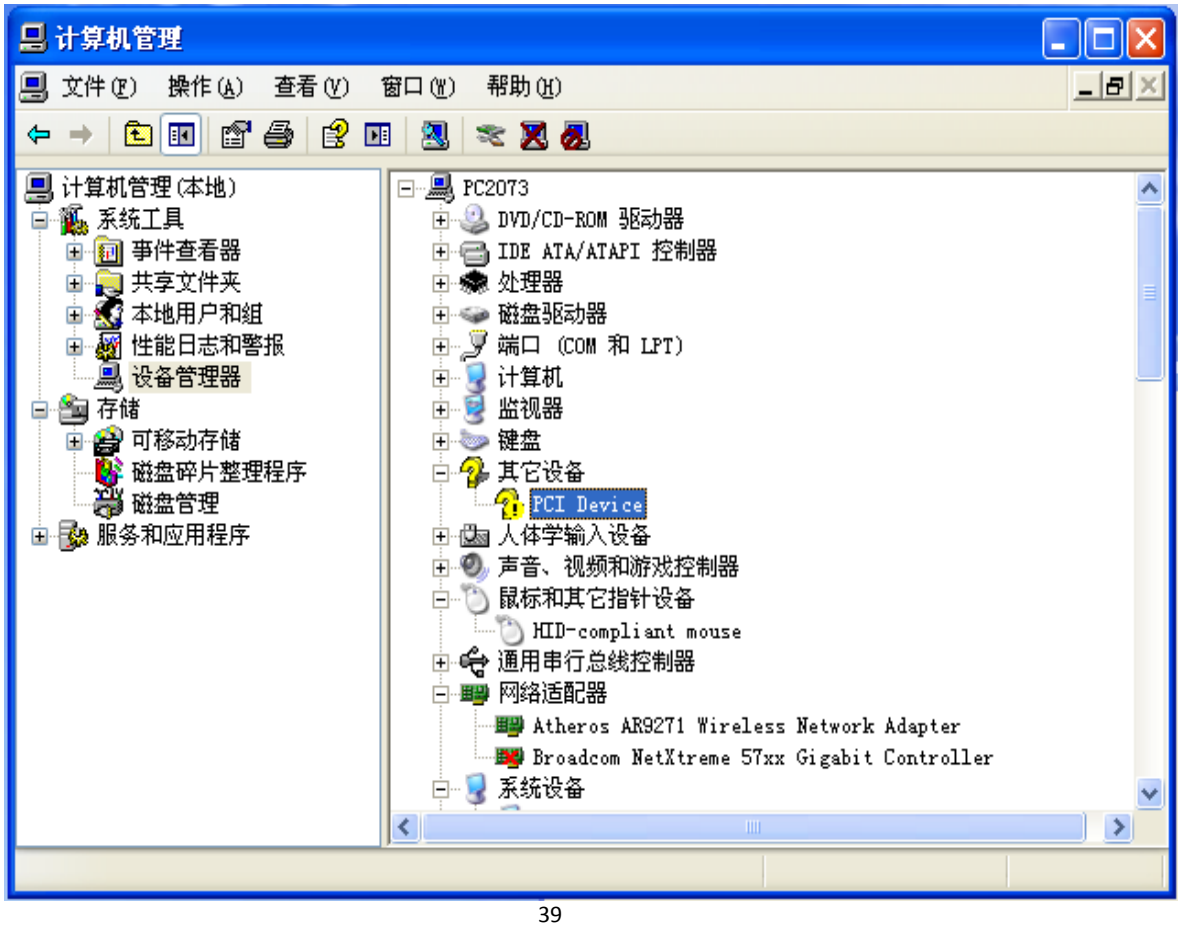
If succeeded, you can see below...



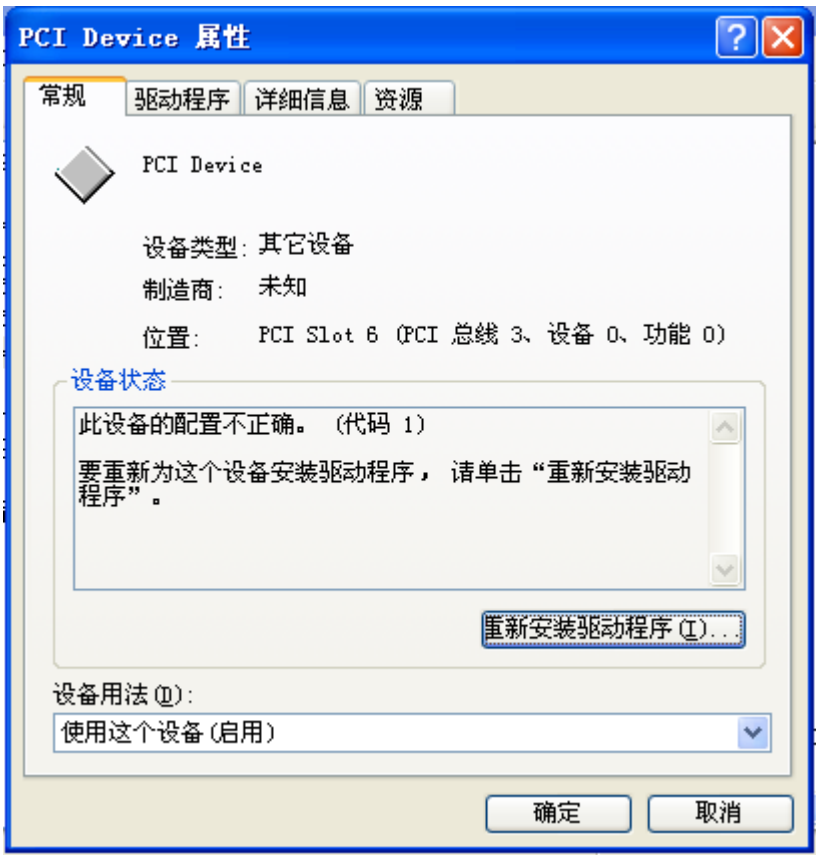
Download “top.sof” into the main board



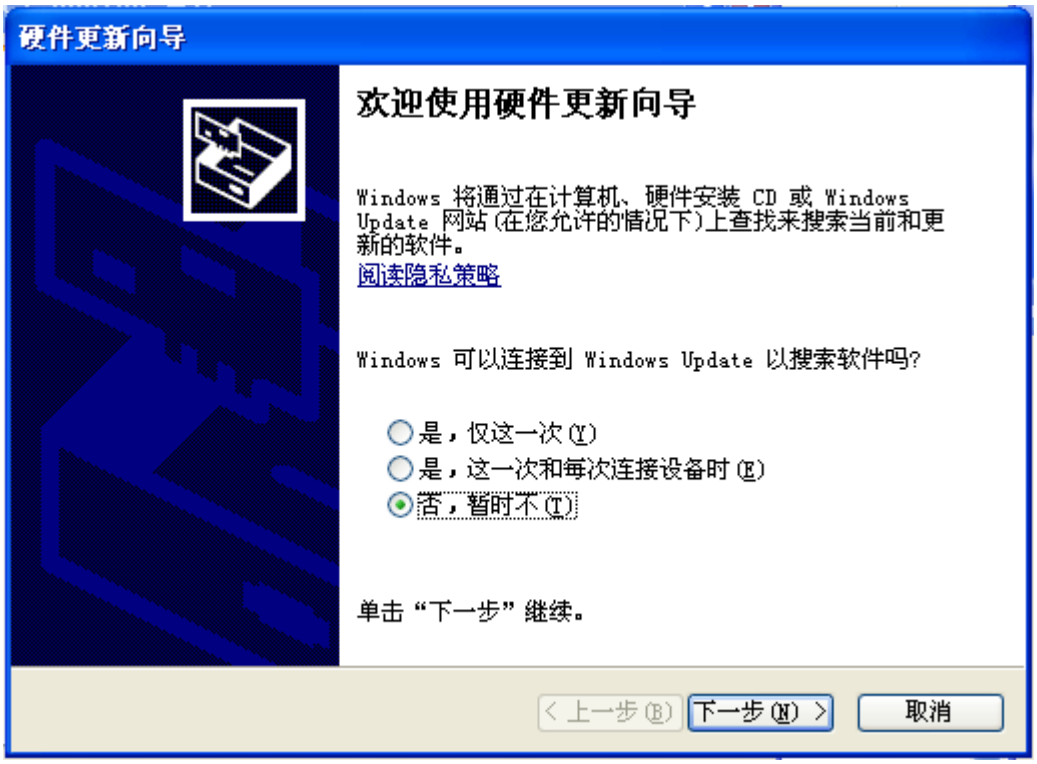
Plug the main board into computer ExpressCard socket。If needed, please using the PCIe Expresscard adapter. After soft restart the computer, you can find the new device in the device list.



Double click the new PCI device

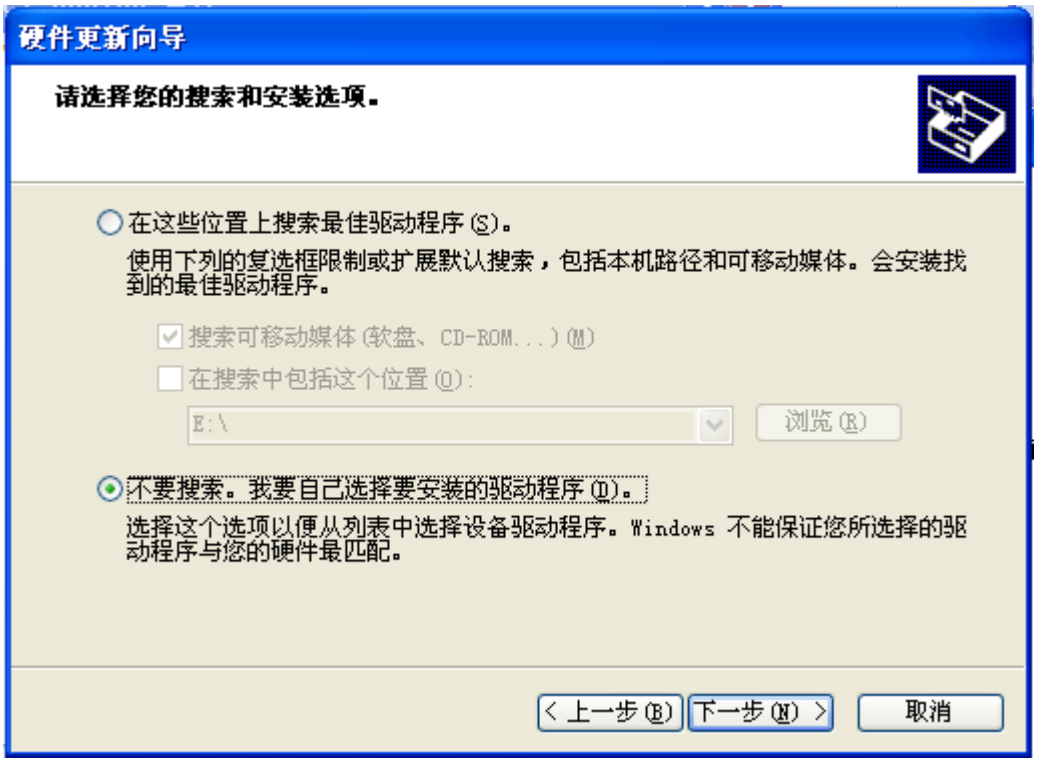


Click to reinstall the driver. Select “No…”, then click “Next”.



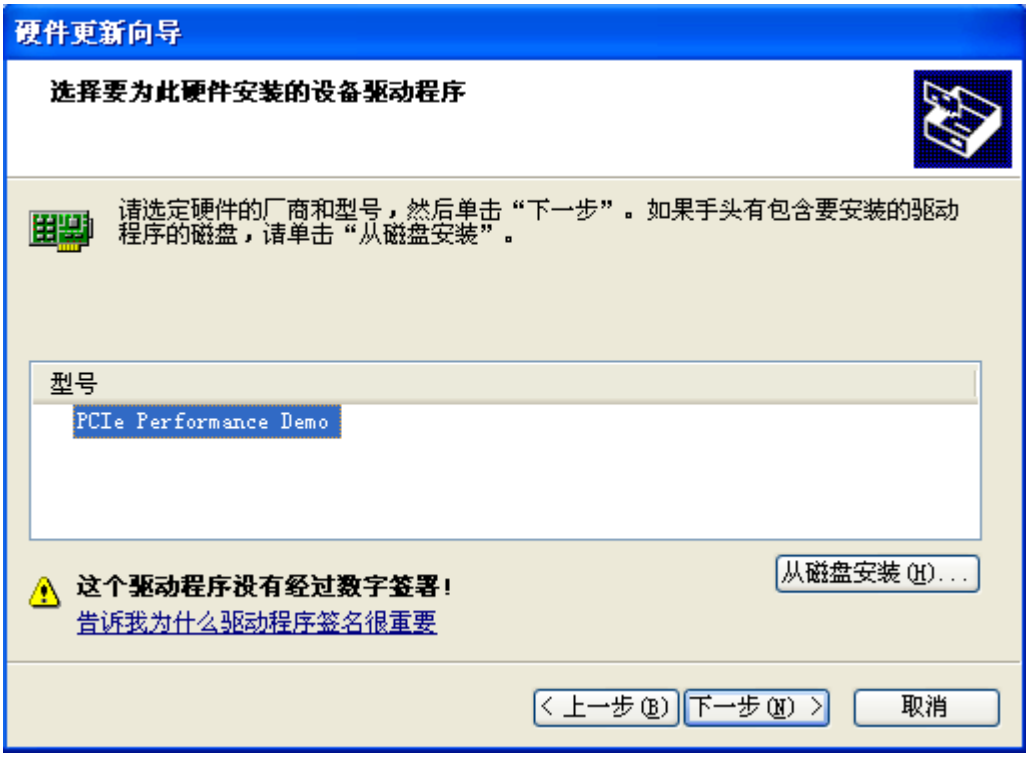
Select choose from manual directory as below and click “Next”

Select as below and click “Next”

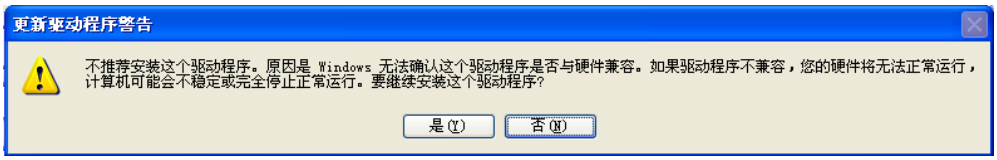


Select “Jungo” from hardware type, then click “Next”.

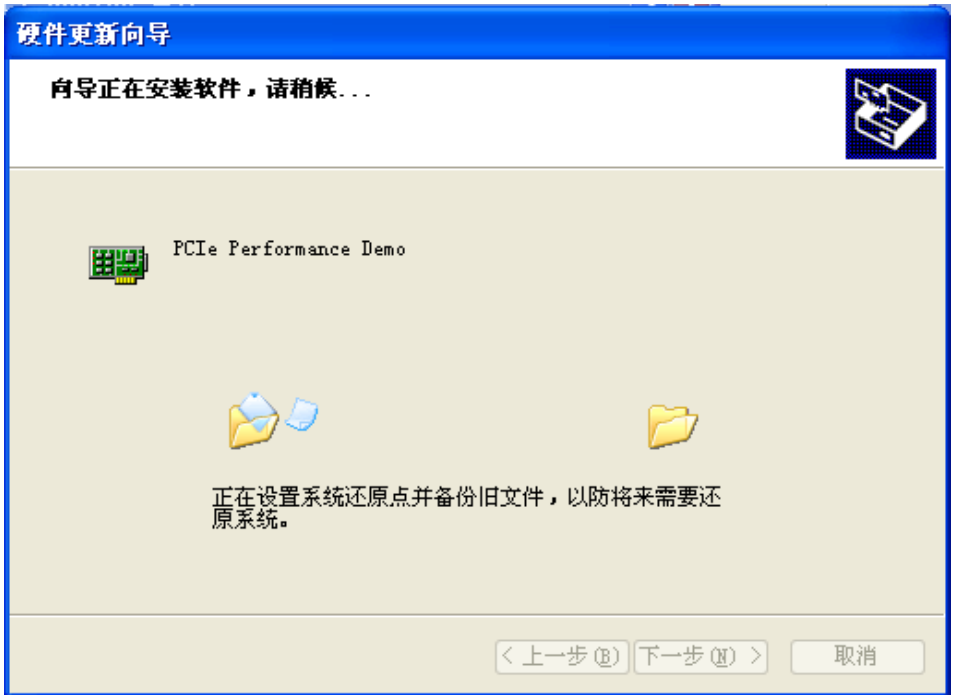
Confirm “PCIe Performance Demo”, click Next



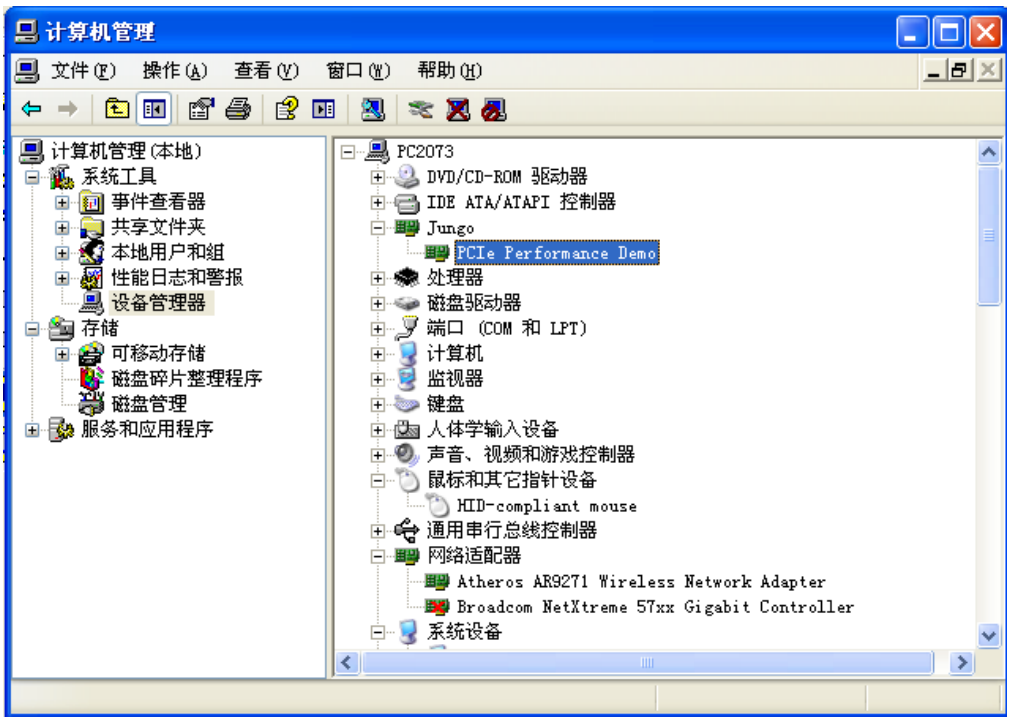
Select “Yes” for warning message.



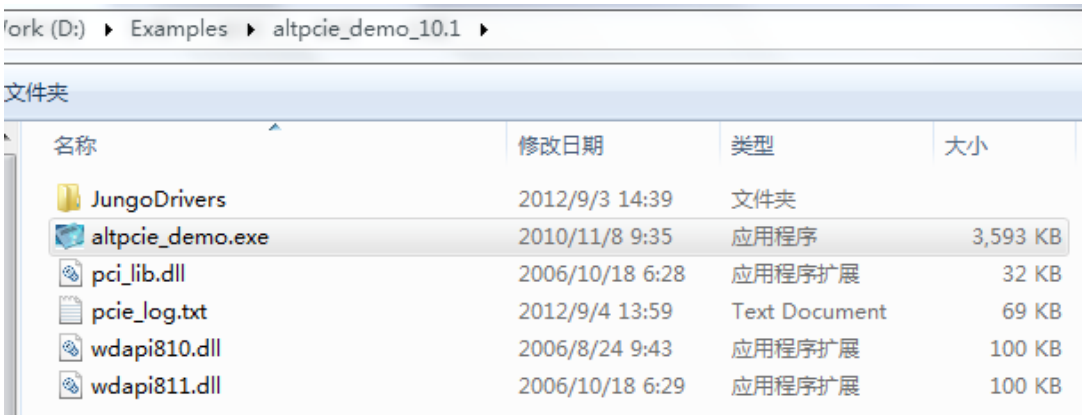
Jungle PCIe driver will be installing.....



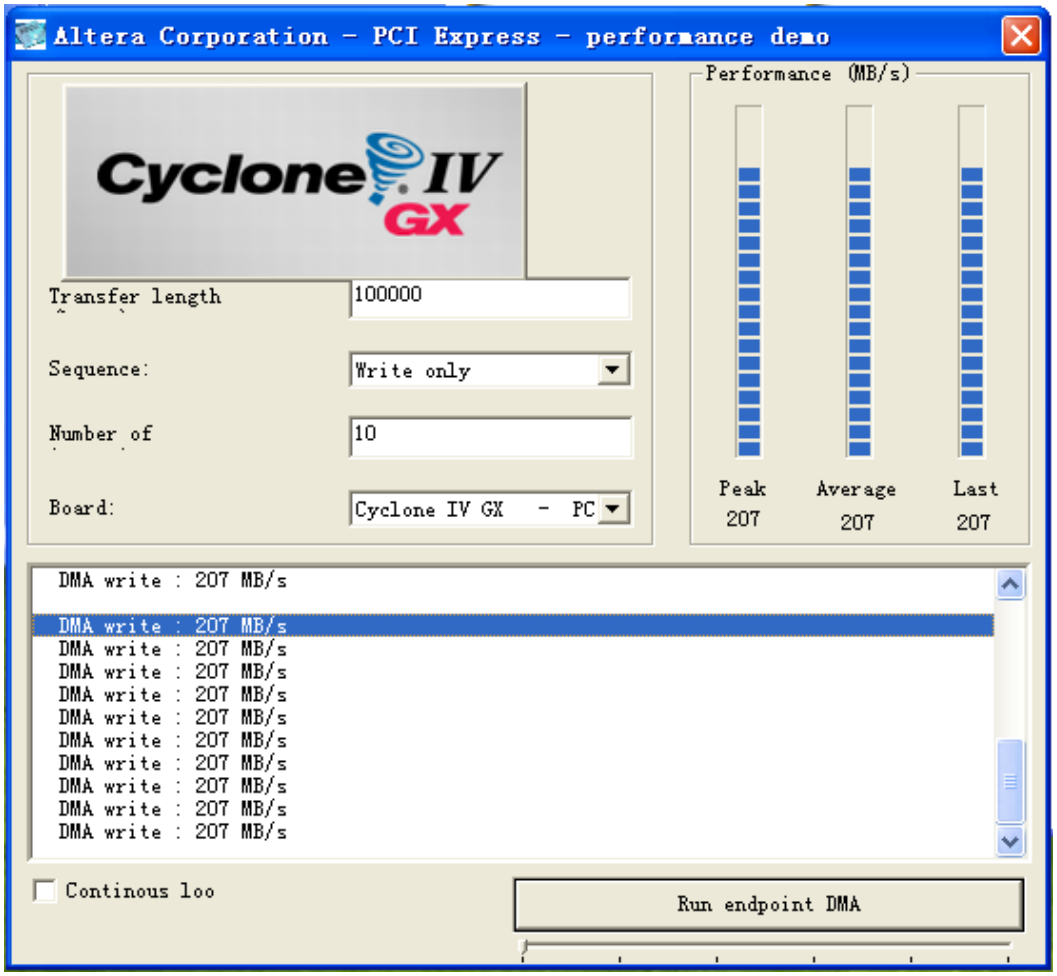
Driver installed successfully.



Run the program below：



Run endpoint DMA



5 Appendix

AN 456: PCI Express High Performance Reference Design - Altera
www.altera.com/literature/an/an456.pdf